TEXAS INSTRUMENTS

AHC/AHCT Logic

Advanced High-Speed CMOS

Data Book

1996 Advanced System Logic Products

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AHC/AHCT Logic
Advanced High-Speed CMOS
Data Book

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INTRODUCTION

The Advanced High-speed CMOS (AHC) logic family provides a natural migration for HCMOS users who need more speed for low-power, low-noise, and low-drive applications. The AHC logic family consists of basic gates, medium-scale integrated circuits, and octal functions fabricated using the EPIC1-S process that produces high performance at low cost.

Performance characteristics of the AHC family are:

- Speed – With typical propagation delays of 5.2 ns (octals), which is about three times faster than HC devices, AHC devices are the quick and quiet solution for higher-speed operation.
- Low noise – The AHC family allows designers to combine the low-noise characteristics of HCMOS devices with today's performance levels without the overshoot/undershoot problems typical of higher-drive devices usually required to get AHC speeds.
- Low power – The AHC family, by using CMOS technology, exhibits low power consumption (40-μA maximum static current, half that of HCMOS).
- Drive – Output drive current is ±8 mA at 5-V V_{CC} and ±4 mA at 3.3-V V_{CC}.
- Packaging – AHC devices are available in D and DW (SOIC), DB (SSOP), N (PDIP), and PW (TSSOP) packages. Selected AHC devices are available in military versions (SN54AHCxx).

Using Texas Instruments (TI) products offers several business advantages:

- Competitive avantage – AHC and VHC devices have equivalent specifications; therefore, AHC devices are "drop in" replaceable. With TI's production capacity, delivery performance, and competitive prices, AHC devices are among the most economical, easy-to-use, and easy-to-get logic products.
- Alternate source – TI has arrangements for one or more alternate sources for AHC devices.

For more information on these and other products, including availability dates, pricing, and final timing specifications, please contact your local Texas Instruments representative, authorized distributor, visit the TI home page at http://www.ti.com, or contact the European Product Information Center at:

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INTRODUCTION

These symbols, terms, and definitions are in accordance with those currently agreed upon by the JEDEC Council of the Electronic Industries Association (EIA) for use in the USA and by the International Electrotechnical Commission (IEC) for international use.

operating conditions and characteristics (in sequence by letter symbols)

C_i Input capacitance

The internal capacitance at an input of the device

C_o Output capacitance

The internal capacitance at an output of the device

C_{pd} Power dissipation capacitance

Used to determine the no-load dynamic power dissipation per logic function (see individual circuit pages): $P_D = C_{pd} V_{CC}^2 f + I_{CC} V_{CC}$

f_{max} Maximum clock frequency

The highest rate at which the clock input of a bistable circuit can be driven through its required sequence while maintaining stable transitions of logic level at the output with input conditions established that should cause changes of output logic level in accordance with the specification

I_{CC} Supply current

The current into* the V_{CC} supply terminal of an integrated circuit

ΔI_{CC} Supply current change

The increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}

I_{CEX} Output high leakage current

The maximum leakage current into the collector of the pulldown output transistor when the output is high and the output forcing condition $V_O = 5.5$ V

$I_{I(hold)}$ Input hold current

Input current that holds the input at the previous state when the driving device goes to a high-impedance state

I_{IH} High-level input current

The current into* an input when a high-level voltage is applied to that input

I_{IL} Low-level input current

The current into* an input when a low-level voltage is applied to that input

I_{off} Input/output power-off leakage current

The maximum leakage current into/out of the input/output transistors when forcing the input/output to 4.5 V and $V_{CC} = 0$ V

I_{OH} High-level output current

The current into* an output with input conditions applied that, according to the product specification, will establish a high level at the output.

I_{OL} Low-level output current

The current into* an output with input conditions applied that, according to the product specification, will establish a low level at the output.

*Current out of a terminal is given as a negative value.

I_{OZ} **Off-state (high-impedance-state) output current (of a 3-state output)**

The current flowing into* an output having 3-state capability with input conditions established that, according to the product specification, will establish the high-impedance state at the output.

t_a **Access time**

The time interval between the application of a specified input pulse and the availability of valid signals at an output

t_c **Clock cycle time**

Clock cycle time is $1/f_{max}$.

t_{dis} **Disable time (of a 3-state or open-collector output)**

The propagation time between the specified reference points on the input and output voltage waveforms with the output changing from either of the defined active levels (high or low) to a high-impedance (off) state

NOTE: For 3-state outputs, $t_{dis} = t_{PHZ}$ or t_{PLZ}. Open-collector outputs will change only if they are low at the time of disabling, so $t_{dis} = t_{PLH}$.

t_{en} **Enable time (of a 3-state or open-collector output)**

The propagation time between the specified reference points on the input and output voltage waveforms with the output changing from a high-impedance (off) state to either of the defined active levels (high or low)

NOTE: In the case of memories, this is the access time from an enable input (e.g., $\overline{OE}$). For 3-state outputs, $t_{en} = t_{PZH}$ or t_{PZL}. Open-collector outputs will change only if they are responding to data that would cause the output to go low, so $t_{en} = t_{PHL}$.

t_h **Hold time**

The time interval during which a signal is retained at a specified input terminal after an active transition occurs at another specified input terminal

NOTES: 1. The hold time is the actual time interval between two signal events and is determined by the system in which the digital circuit operates. A minimum value is specified that is the shortest interval for which correct operation of the digital circuit is to be expected.

2. The hold time may have a negative value in which case the minimum limit defines the longest interval (between the release of the signal and the active transition) for which correct operation of the digital circuit is to be expected.

t_{pd} **Propagation delay time**

The time between the specified reference points on the input and output voltage waveforms with the output changing from one defined level (high or low) to the other defined level ($t_{pd} = t_{PHL}$ or t_{PLH})

t_{PHL} **Propagation delay time, high-to-low level output**

The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined high level to the defined low level

t_{PHZ} **Disable time (of a 3-state output) from high level**

The time interval between the specified reference points on the input and the output voltage waveforms with the 3-state output changing from the defined high level to the high-impedance (off) state

t_{PLH} **Propagation delay time, low-to-high level output**

The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined low level to the defined high level

*Current out of a terminal is given as a negative value.

t_{PLZ} **Disable time (of a 3-state output) from low level**

The time interval between the specified reference points on the input and the output voltage waveforms with the 3-state output changing from the defined low level to the high-impedance (off) state

t_{PZH} **Enable time (of a 3-state output) to high level**

The time interval between the specified reference points on the input and output voltage waveforms with the 3-state output changing from the high-impedance (off) state to the defined high level

t_{PZL} **Enable time (of a 3-state output) to low level**

The time interval between the specified reference points on the input and output voltage waveforms with the 3-state output changing from the high-impedance (off) state to the defined low level

t_{su} **Setup time**

The time interval between the application of a signal at a specified input terminal and a subsequent active transition at another specified input terminal

NOTES: 1. The setup time is the actual time interval between two signal events and is determined by the system in which the digital circuit operates. A minimum value is specified that is the shortest interval for which correct operation of the digital circuit is guaranteed.

2. The setup time may have a negative value, in which case the minimum limit defines the longest interval (between the active transition and the application of the other signal) for which correct operation of the digital circuit is guaranteed.

t_w **Pulse duration (width)**

The time interval between specified reference points on the leading and trailing edges of the pulse waveform

V_{IH} **High-level input voltage**

An input voltage within the more positive (less negative) of the two ranges of values used to represent the binary variables

NOTE: A minimum is specified that is the least-positive value of high-level input voltage for which operation of the logic element within specification limits is to be expected.

V_{IL} **Low-level input voltage**

An input voltage within the less positive (more negative) of the two ranges of values used to represent the binary variables

NOTE: A maximum is specified that is the most-positive value of low-level input voltage for which operation of the logic element within specification limits is to be expected.

V_{OH} **High-level output voltage**

The voltage at an output terminal with input conditions applied that, according to product specification, will establish a high level at the output

V_{OL} **Low-level output voltage**

The voltage at an output terminal with input conditions applied that, according to product specification, will establish a low level at the output

V_{IT+} **Positive-going input threshold level**

The voltage level at a transition-operated input that causes operation of the logic element according to specification as the input voltage rises from a level below the negative-going threshold voltage, V_{IT-}

V_{IT-} **Negative-going input threshold level**

The voltage level at a transition-operated input that causes operation of the logic element according to specification as the input voltage falls from a level above the positive-going threshold voltage, V_{IT+}

EXPLANATION OF FUNCTION TABLES

The following symbols are used in function tables on TI data sheets:

H	=	high level (steady state)
L	=	low level (steady state)
↑	=	transition from low to high level
↓	=	transition from high to low level
→	=	value/level or resulting value/level is routed to indicated destination
↶	=	value/level is re-entered
X	=	irrelevant (any input, including transitions)
Z	=	off (high-impedance) state of a 3-state output
a . . . h	=	the level of steady-state inputs A through H, respectively
Q_0	=	level of Q before the indicated steady-state input conditions were established
$\overline{Q}_0$	=	complement of Q_0 or level of $\overline{Q}$ before the indicated steady-state input conditions were established
Q_n	=	level of Q before the most recent active transition indicated by ↓ or ↑
⎍	=	one high-level pulse
⎴	=	one low-level pulse
Toggle	=	each output changes to the complement of its previous level on each active transition indicated by ↓ or ↑

If, in the input columns, a row contains only the symbols H, L, and/or X, this means the indicated output is valid whenever the input configuration is achieved and regardless of the sequence in which it is achieved. The output persists so long as the input configuration is maintained.

If, in the input columns, a row contains H, L, and/or X together with ↑ and/or ↓, this means the output is valid whenever the input configuration is achieved but the transition(s) must occur following the achievement of the steady-state levels. If the output is shown as a level (H, L, Q_0, or $\overline{Q}_0$), it persists so long as the steady-state input levels and the levels that terminate indicated transitions are maintained. Unless otherwise indicated, input transitions in the opposite direction to those shown have no effect at the output. (If the output is shown as a pulse, ⎍ or ⎴, the pulse follows the indicated input transition and persists for an interval dependent on the circuit.)

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Among the most complex function tables are those of the shift registers. These embody most of the symbols used in any of the function tables, plus more. Below is the function table of a 4-bit bidirectional universal shift register, e.g., type SN74194.

FUNCTION TABLE

INPUTS										OUTPUTS			
CLEAR	MODE		CLOCK	SERIAL		PARALLEL				Q_A	Q_B	Q_C	Q_D
	S1	S0		LEFT	RIGHT	A	B	C	D				
L	X	X	X	X	X	X	X	X	X	L	L	L	L
H	X	X	L	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
H	H	H	↑	X	X	a	b	c	d	a	b	c	d
H	L	H	↑	X	H	H	H	H	H	H	Q_{An}	Q_{Bn}	Q_{Cn}
H	L	H	↑	X	L	L	L	L	L	L	Q_{An}	Q_{Bn}	Q_{Cn}
H	H	L	↑	H	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	H
H	H	L	↑	L	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	L
H	L	L	X	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}

The first line of the table represents a synchronous clearing of the register and says that if clear is low, all four outputs will be reset low regardless of the other inputs. In the following lines, clear is inactive (high) and so has no effect.

The second line shows that so long as the clock input remains low (while clear is high), no other input has any effect and the outputs maintain the levels they assumed before the steady-state combination of clear high and clock low was established. Since on other lines of the table only the rising transition of the clock is shown to be active, the second line implicitly shows that no further change in the outputs will occur while the clock remains high or on the high-to-low transition of the clock.

The third line of the table represents synchronous parallel loading of the register and says that if S1 and S0 are both high then, without regard to the serial input, the data entered at A will be at output Q_A, data entered at B will be at Q_B, and so forth, following a low-to-high clock transition.

The fourth and fifth lines represent the loading of high- and low-level data, respectively, from the shift-right serial input and the shifting of previously entered data one bit; data previously at Q_A is now at Q_B, the previous levels of Q_B and Q_C are now at Q_C and Q_D, respectively, and the data previously at Q_D is no longer in the register. This entry of serial data and shift takes place on the low-to-high transition of the clock when S1 is low and S0 is high and the levels at inputs A through D have no effect.

The sixth and seventh lines represent the loading of high- and low-level data, respectively, from the shift-left serial input and the shifting of previously entered data one bit; data previously at Q_B is now at Q_A, the previous levels of Q_C and Q_D are now at Q_B and Q_C, respectively, and the data previously at Q_A is no longer in the register. This entry of serial data and shift takes place on the low-to-high transition of the clock when S1 is high and S0 is low and the levels at inputs A through D have no effect.

The last line shows that as long as both inputs are low, no other input has any effect and, as in the second line, the outputs maintain the levels they assumed before the steady-state combination of clear high and both mode inputs low was established.

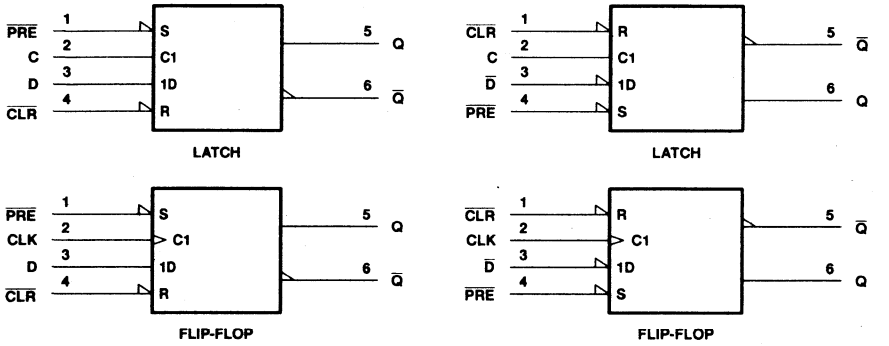
The function table functional tests do not reflect all possible combinations or sequential modes.

D FLIP-FLOP AND LATCH SIGNAL CONVENTIONS

It is normal TI practice to name the outputs and other inputs of a D-type flip-flop or latch and to draw its logic symbol based on the assumption of true data (D) inputs. Outputs that produce data in phase with the data inputs are called Q and those producing complementary data are called $\overline{Q}$. An input that causes a Q output to go high or a $\overline{Q}$ output to go low is called preset ($\overline{PRE}$). An input that causes a $\overline{Q}$ output to go high or a Q output to go low is called clear ($\overline{CLR}$). Bars are used over these pin names ($\overline{PRE}$ and $\overline{CLR}$) if they are active low.

The devices on several data sheets are second-source designs, and the pin name conventions used by the original manufacturers have been retained. That makes it necessary to designate the inputs and outputs of the inverting circuits $\overline{D}$ and Q.

In some applications, it may be advantageous to redesignate the data input from D to $\overline{D}$ or vice versa. In that case, all the other inputs and outputs should be renamed as shown below. Also shown are corresponding changes in the graphical symbols. Arbitrary pin numbers are shown.



The figures show that when Q and $\overline{Q}$ exchange names, the preset and clear pins also exchange names. The polarity indicators (⊾) on $\overline{PRE}$ and $\overline{CLR}$ remain, as these inputs are still active low, but the presence or absence of the polarity indicator changes at D (or $\overline{D}$), Q, and $\overline{Q}$. Pin 5 (Q or $\overline{Q}$) is still in phase with the data input (D or $\overline{D}$); their active levels change together.

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In digital system design, consideration must be given to thermal management of components. The small size of the small-outline package makes this even more critical. Figure 1 shows the thermal resistance of these packages for various rates of air flow.

The thermal resistances in Figure 1 can be used to approximate typical and maximum virtual junction temperatures. In general, the junction temperature for any device can be calculated using the following equation:

$$T_J = R_{\theta JA} \times P_T + T_A$$

Where:

T_J = virtual junction temperature
$R_{\theta JA}$ = thermal resistance, junction to free air
P_T = total power dissipation of the device
T_A = free-air temperature

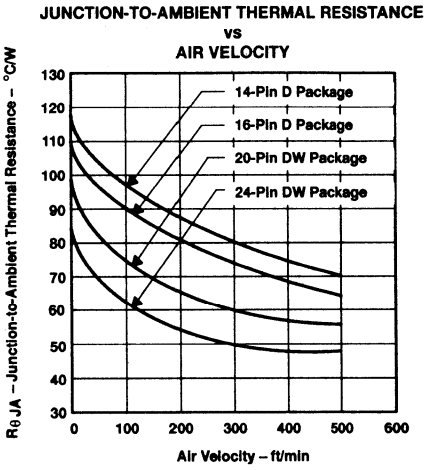

Figure 1

Derating curves for 210-mil shrink small-outline package are shown in Figures 2 through 5.

DERATING CURVES FOR 210-MIL SHRINK SMALL-OUTLINE PACKAGE (DB)

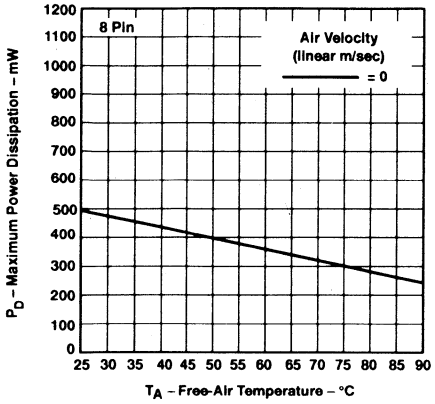

Figure 2

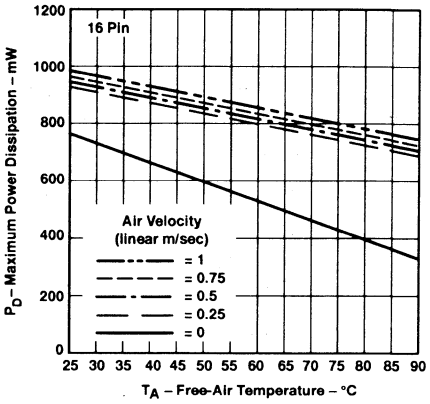

Figure 3

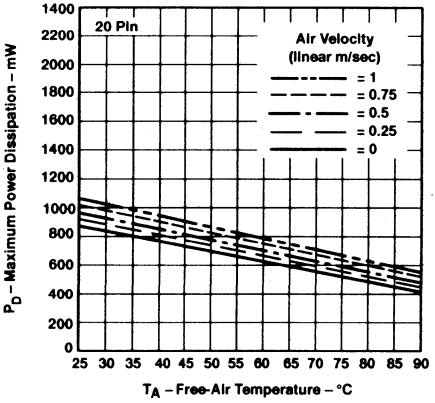

Figure 4

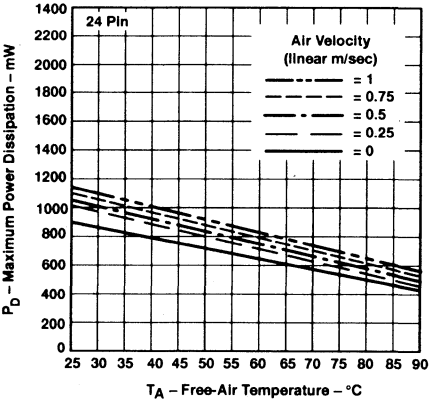

Figure 5

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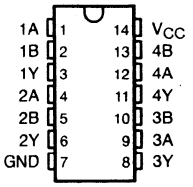
- **Operating Range: 2-V to 5.5-V V_{CC}**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **High Latch-Up Immunity Exceeds 300 mA Per JEDEC Standard JESD-17**
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW) Packages, and Standard Plastic (N) DIPs**

D, DB, N, OR PW PACKAGE
(TOP VIEW)



description

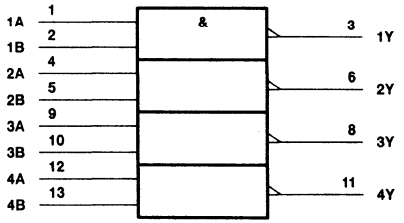
The SN74AHC00 performs the Boolean functions $Y = \overline{A \bullet B}$ or $Y = \overline{A} + \overline{B}$ in positive logic.

The SN74AHC00 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each gate)

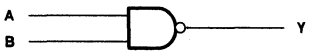
INPUTS		OUTPUT
A	B	Y
H	H	L
L	X	H
X	L	H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram, each gate (positive logic)



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... –0.5 V to 7 V
Output voltage range, V_O (see Note 1) ..... –0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$) ..... –20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±25 mA
Continuous current through V_{CC} or GND ..... ±50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2): D package ..... 1.25 W
DB or PW package ..... 0.5 W
N package ..... 1.1 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions (see Note 3)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5		V
		V_{CC} = 3 V	2.1		
		V_{CC} = 5.5 V	3.85		
V_{IL}	Low-level input voltage	V_{CC} = 2 V		0.5	V
		V_{CC} = 3 V		0.9	
		V_{CC} = 5.5 V		1.65	
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2 V		–50	μA
		V_{CC} = 3.3 V ± 0.3 V		–4	mA
		V_{CC} = 5 V ± 0.5 V		–8	
I_{OL}	Low-level output current	V_{CC} = 2 V		50	μA
		V_{CC} = 3.3 V ± 0.3 V		4	mA
		V_{CC} = 5 V ± 0.5 V		8	
$\Delta t/\Delta v$	Input transition rise or fall rate	V_{CC} = 3.3 V ± 0.3 V		100	ns/V
		V_{CC} = 5 V ± 0.5 V		20	
T_A	Operating free-air temperature		–40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC}	T_A = 25°C			MIN	MAX	UNIT
					MIN	TYP	MAX			
V_{OH}		I_{OH} = –50 μA		2 V	1.9	2		1.9		V
				3 V	2.9	3		2.9		
				4.5 V	4.4	4.5		4.4		
		I_{OH} = –4 mA		3 V	2.58			2.48		
		I_{OH} = –8 mA		4.5 V	3.94			3.8		
V_{OL}		I_{OL} = 50 μA		2 V			0.1		0.1	V
				3 V			0.1		0.1	
				4.5 V			0.1		0.1	
		I_{OL} = 4 mA		3 V			0.36		0.44	
		I_{OL} = 8 mA		4.5 V			0.36		0.44	
I_I	A or B inputs	$V_I = V_{CC}$ or GND		5.5 V			±0.1		±1	μA
I_{CC}		$V_I = V_{CC}$ or GND,	I_O = 0	5.5 V			2		20	μA
C_i		$V_I = V_{CC}$ or GND		5 V		2	10		10	pF

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
t_{PLH}	A or B	Y	C_L = 15 pF		5.5	7.9	1	9.5	ns
t_{PHL}					5.5	7.9	1	9.5	
t_{PLH}	A or B	Y	C_L = 50 pF		8	11.4	1	13	ns
t_{PHL}					8	11.4	1	13	

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
t_{PLH}	A or B	Y	C_L = 15 pF		3.7	5.5	1	6.5	ns
t_{PHL}					3.7	5.5	1	6.5	
t_{PLH}	A or B	Y	C_L = 50 pF		5.2	7.5	1	8.5	ns
t_{PHL}					5.2	7.5	1	8.5	

noise characteristics, V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C (see Note 4)

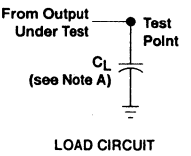
PARAMETER		MIN	TYP	MAX	UNIT
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.3	0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		–0.3	–0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}		4.6		V
$V_{IH(D)}$	High-level dynamic input voltage	3.5			V
$V_{IL(D)}$	Low-level dynamic input voltage			1.5	V

NOTE 4: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

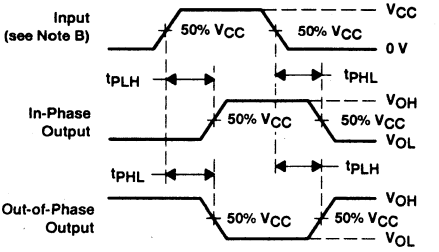
operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	C_L = 50 pF, f = 1 MHz	9.5	pF

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



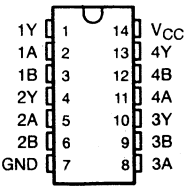
VOLTAGE WAVEFORMS
DELAY TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

- **Operating Range: 2-V to 5.5-V V_{CC}**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW) Packages, and Standard Plastic (N) DIPs**

D, DB, N, OR PW PACKAGE
(TOP VIEW)



description

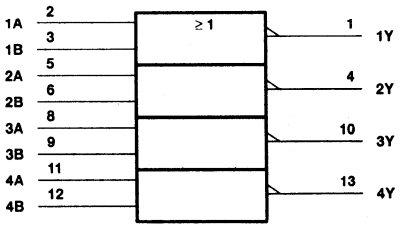
This device contains four independent 2-input NOR gates that perform the Boolean functions $Y = \overline{A} \cdot \overline{B}$ or $Y = \overline{A + B}$ in positive logic.

The SN74AHC02 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each gate)

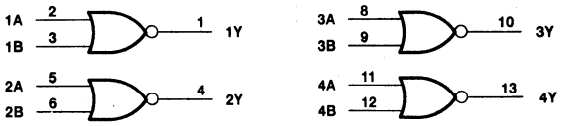
INPUTS		OUTPUT
A	B	Y
H	X	L
X	H	L
L	L	H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



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PRODUCT PREVIEW

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$) ..... −20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±25 mA
Continuous current through V_{CC} or GND ..... ±50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2): D package ..... 1.25 W
DB or PW package ..... 0.5 W
N package ..... 1.1 W
Storage temperature range, T_{stg} ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

PRODUCT PREVIEW

recommended operating conditions (see Note 3)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5		V
		V_{CC} = 3 V	2.1		
		V_{CC} = 5.5 V	3.85		
V_{IL}	Low-level input voltage	V_{CC} = 2 V		0.5	V
		V_{CC} = 3 V		0.9	
		V_{CC} = 5.5 V		1.65	
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2 V		−50	μA
		V_{CC} = 3.3 V ± 0.3 V		−4	mA
		V_{CC} = 5 V ± 0.5 V		−8	
I_{OL}	Low-level output current	V_{CC} = 2 V		50	μA
		V_{CC} = 3.3 V ± 0.3 V		4	mA
		V_{CC} = 5 V ± 0.5 V		8	
$\Delta t/\Delta v$	Input transition rise or fall rate	V_{CC} = 3.3 V ± 0.3 V		100	ns/V
		V_{CC} = 5 V ± 0.5 V		20	
T_A	Operating free-air temperature		−40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
V_{OH}	I_{OH} = –50 μA	2 V	1.9	2		1.9		V
		3 V	2.9	3		2.9		
		4.5 V	4.4	4.5		4.4		
	I_{OH} = –4 mA	3 V	2.58			2.48		
	I_{OH} = –8 mA	4.5 V	3.94			3.8		
V_{OL}	I_{OL} = 50 μA	2 V			0.1		0.1	V
		3 V			0.1		0.1	
		4.5 V			0.1		0.1	
	I_{OL} = 4 mA	3 V			0.36		0.44	
	I_{OL} = 8 mA	4.5 V			0.36		0.44	
I_I	V_I = V_{CC} or GND	5.5 V			±0.1		±1	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			2		20	μA
C_i	V_I = V_{CC} or GND	5 V		4	10		10	pF

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
t_{PLH}	A or B	Y	C_L = 15 pF		5.6	7.9	1	9.5	ns
t_{PHL}					5.6	7.9	1	9.5	
t_{PLH}	A or B	Y	C_L = 50 pF		8.1	11.4	1	13	ns
t_{PHL}					8.1	11.4	1	13	

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
t_{PLH}	A or B	Y	C_L = 15 pF		3.6	5.5	1	6.5	ns
t_{PHL}					3.6	5.5	1	6.5	
t_{PLH}	A or B	Y	C_L = 50 pF		5.1	7.5	1	8.5	ns
t_{PHL}					5.1	7.5	1	8.5	

noise characteristics, V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C (see Note 4)

PARAMETER		MIN	TYP	MAX	UNIT
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}			0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}			–0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}				V
$V_{IH(D)}$	High-level dynamic input voltage	3.5			V
$V_{IL(D)}$	Low-level dynamic input voltage			1.5	V

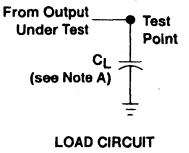
NOTE 4: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

PRODUCT PREVIEW

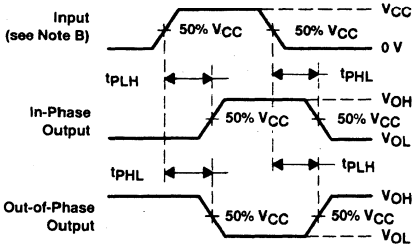
operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per gate	C_L = 50 pF, f = 1 MHz	15	pF

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



VOLTAGE WAVEFORMS
DELAY TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

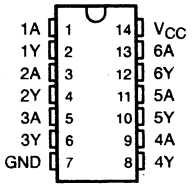
Figure 1. Load Circuit and Voltage Waveforms

PRODUCT PREVIEW

SCLS231B – OCTOBER 1995 – REVISED JANUARY 1996

- **Operating Range: 2-V to 5.5-V V_{CC}**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **High Latch-Up Immunity Exceeds 300 mA Per JEDEC Standard JESD-17**
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW) Packages, and Standard Plastic (N) DIPs**

D, DB, N, OR PW PACKAGE
(TOP VIEW)



description

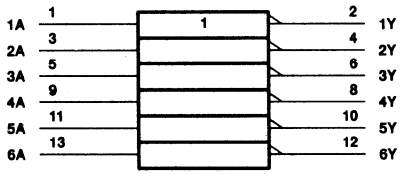
The SN74AHC04 contains six independent inverters. The device performs the Boolean function $Y = \overline{A}$.

The SN74AHC04 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each inverter)

INPUT A	OUTPUT Y
H	L
L	H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0) ..... − 20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ± 20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ± 25 mA
Continuous current through V_{CC} or GND ..... ± 50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2): D package ..... 1.25 W
DB or PW package ..... 0.5 W
N package ..... 1.1 W
Storage temperature range, T_{stg} ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions (see Note 3)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5		V
		V_{CC} = 3 V	2.1		
		V_{CC} = 5.5 V	3.85		
V_{IL}	Low-level input voltage	V_{CC} = 2 V		0.5	V
		V_{CC} = 3 V		0.9	
		V_{CC} = 5.5 V		1.65	
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2 V		− 50	μA
		V_{CC} = 3.3 V ± 0.3 V		− 4	mA
		V_{CC} = 5 V ± 0.5 V		− 8	
I_{OL}	Low-level output current	V_{CC} = 2 V		50	μA
		V_{CC} = 3.3 V ± 0.3 V		4	mA
		V_{CC} = 5 V ± 0.5 V		8	
$\Delta t/\Delta v$	Input transition rise or fall rate	V_{CC} = 3.3 V ± 0.3 V		100	ns/V
		V_{CC} = 5 V ± 0.5 V		20	
T_A	Operating free-air temperature		− 40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
V_{OH}	I_{OH} = – 50 μA	2 V	1.9	2		1.9		V
		3 V	2.9	3		2.9		
		4.5 V	4.4	4.5		4.4		
	I_{OH} = –4 mA	3 V	2.58			2.48		
	I_{OH} = – 8 mA	4.5 V	3.94			3.8		
V_{OL}	I_{OL} = 50 μA	2 V			0.1		0.1	V
		3 V			0.1		0.1	
		4.5 V			0.1		0.1	
	I_{OL} = 4 mA	3 V			0.36		0.44	
	I_{OL} = 8 mA	4.5 V			0.36		0.44	
I_I	V_I = V_{CC} or GND	5.5 V			± 0.1		± 1	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			2		20	μA
C_i	V_I = V_{CC} or GND	5 V		2	10		10	pF

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
t_{PLH}	A	Y	C_L = 15 pF		5	7.1	1	8.5	ns
t_{PHL}					5	7.1	1	8.5	
t_{PLH}	A	Y	C_L = 50 pF		7.5	10.6	1	12	ns
t_{PHL}					7.5	10.6	1	12	

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
t_{PLH}	A	Y	C_L = 15 pF		3.8	5.5	1	6.5	ns
t_{PHL}					3.8	5.5	1	6.5	
t_{PLH}	A	Y	C_L = 50 pF		5.3	7.5	1	8.5	ns
t_{PHL}					5.3	7.5	1	8.5	

noise characteristics, V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C (see Note 4)

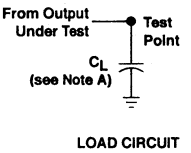
PARAMETER		MIN	TYP	MAX	UNIT
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.4		V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		–0.4		V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}		4.8		V
$V_{IH(D)}$	High-level dynamic input voltage	3.5			V
$V_{IL(D)}$	Low-level dynamic input voltage			1.5	V

NOTE 4: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

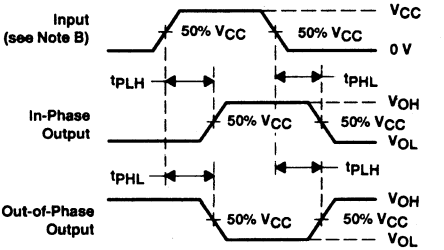
operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	C_L = 50 pF, f = 1 MHz	12	pF

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



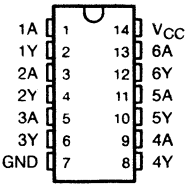
VOLTAGE WAVEFORMS
DELAY TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

- **Operating Range: 2-V to 5.5-V V_{CC}**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **Unbuffered Outputs**
- **High Latch-Up Immunity Exceeds 300 mA Per JEDEC Standard JESD-17**
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW) Packages, and Standard Plastic (N) DIPs**

D, DB, N, OR PW PACKAGE
(TOP VIEW)



description

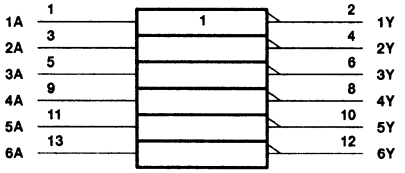
The SN74AHCU04 contains six independent inverters. The device performs the Boolean function $Y = \overline{A}$. Internal circuitry consists of single stage inverters that can be used in analog applications such as crystal oscillators.

The SN74AHCU04 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each inverter)

INPUT A	OUTPUT Y
H	L
L	H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... –0.5 V to 7 V
Output voltage range, V_O (see Note 1) ..... –0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0) ..... –20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±25 mA
Continuous current through V_{CC} or GND ..... ±50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2): D package ..... 1.25 W
DB or PW package ..... 0.5 W
N package ..... 1.1 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions (see Note 3)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.7		V
		V_{CC} = 3 V	2.4		
		V_{CC} = 5.5 V	4.4		
V_{IL}	Low-level input voltage	V_{CC} = 2 V		0.3	V
		V_{CC} = 3 V		0.6	
		V_{CC} = 5.5 V		1.1	
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2 V		–50	μA
		V_{CC} = 3.3 V ± 0.3 V		–4	mA
		V_{CC} = 5 V ± 0.5 V		–8	
I_{OL}	Low-level output current	V_{CC} = 2 V		50	μA
		V_{CC} = 3.3 V ± 0.3 V		4	mA
		V_{CC} = 5 V ± 0.5 V		8	
T_A	Operating free-air temperature		–40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
V_{OH}	I_{OH} = –50 μA	2 V	1.8	2		1.8		V
		3 V	2.7	3		2.7		
		4.5 V	4	4.5		4		
	I_{OH} = –4 mA	3 V	2.58			2.48		
	I_{OH} = –8 mA	4.5 V	3.94			3.8		
V_{OL}	I_{OL} = 50 μA	2 V			0.2		0.2	V
		3 V			0.3		0.3	
		4.5 V			0.5		0.5	
	I_{OL} = 4 mA	3 V			0.36		0.44	
	I_{OL} = 8 mA	4.5 V			0.36		0.44	
I_I	V_I = V_{CC} or GND	5.5 V			±0.1		±1	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			2		20	μA
C_i	V_I = V_{CC} or GND	5 V		2	10		10	pF

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	OUTPUT CAPACITANCE	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
t_{PLH}	A	Y	C_L = 15 pF		5	8.9	1	10.5	ns
t_{PHL}					5	8.9	1	10.5	
t_{PLH}	A	Y	C_L = 50 pF		7.5	11.4	1	13	ns
t_{PHL}					7.5	11.4	1	13	

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	OUTPUT CAPACITANCE	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
t_{PLH}	A	Y	C_L = 15 pF		3.5	5.5	1	6.5	ns
t_{PHL}					3.5	5.5	1	6.5	
t_{PLH}	A	Y	C_L = 50 pF		5	7	1	8	ns
t_{PHL}					5	7	1	8	

noise characteristics, V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C (see Note 4)

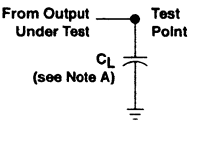
PARAMETER		MIN	TYP	MAX	UNIT
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.5		V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		–0.5		V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}		4.3		V
$V_{IH(D)}$	High-level dynamic input voltage	4			V
$V_{IL(D)}$	Low-level dynamic input voltage			1	V

NOTE 4: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

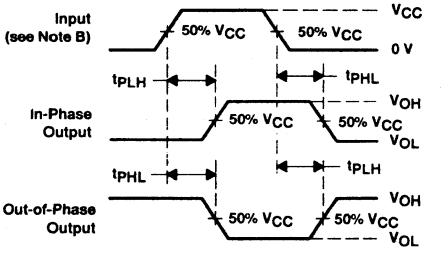
operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	C_L = 50 pF, f = 1 MHz	7.3	pF

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



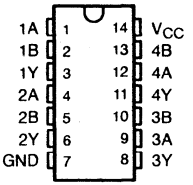
VOLTAGE WAVEFORMS
DELAY TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

- **Operating Range: 2-V to 5.5-V V_{CC}**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **High Latch-Up Immunity Exceeds 300 mA Per JEDEC Standard JESD-17**
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW) Packages, and Standard Plastic (N) DIPs**

D, DB, N, OR PW PACKAGE
(TOP VIEW)



description

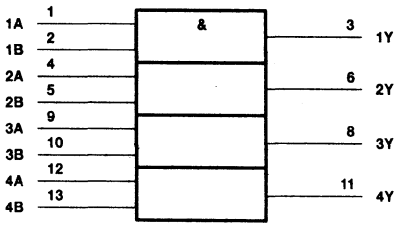
The SN74AHC08 is a quadruple 2-input positive-AND gate. The device performs the Boolean functions $Y = A \bullet B$ or $Y = \overline{\overline{A} + \overline{B}}$ in positive logic.

The SN74AHC08 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each gate)

INPUTS		OUTPUT
A	B	Y
H	H	H
L	X	L
X	L	L

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... –0.5 V to 7 V
Output voltage range, V_O (see Note 1) ..... –0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0) ..... –20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±25 mA
Continuous current through V_{CC} or GND ..... ±50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2): D package ..... 1.25 W
DB or PW package ..... 0.5 W
N package ..... 1.1 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions (see Note 3)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5		V
		V_{CC} = 3 V	2.1		
		V_{CC} = 5.5 V	3.85		
V_{IL}	Low-level input voltage	V_{CC} = 2 V		0.5	V
		V_{CC} = 3 V		0.9	
		V_{CC} = 5.5 V		1.65	
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2 V		–50	μA
		V_{CC} = 3.3 V ± 0.3 V		–4	mA
		V_{CC} = 5 V ± 0.5 V		–8	
I_{OL}	Low-level output current	V_{CC} = 2 V		50	μA
		V_{CC} = 3.3 V ± 0.3 V		4	mA
		V_{CC} = 5 V ± 0.5 V		8	
$\Delta t/\Delta v$	Input transition rise or fall rate	V_{CC} = 3.3 V ± 0.3 V		100	ns/V
		V_{CC} = 5 V ± 0.5 V		20	
T_A	Operating free-air temperature		–40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC}	T_A = 25°C			MIN	MAX	UNIT
					MIN	TYP	MAX			
V_{OH}		I_{OH} = –50 μA		2 V	1.9	2		1.9		V
				3 V	2.9	3		2.9		
				4.5 V	4.4	4.5		4.4		
		I_{OH} = –4 mA		3 V	2.58			2.48		
		I_{OH} = –8 mA		4.5 V	3.94			3.8		
V_{OL}		I_{OL} = 50 μA		2 V			0.1		0.1	V
				3 V			0.1		0.1	
				4.5 V			0.1		0.1	
		I_{OL} = 4 mA		3 V			0.36		0.44	
		I_{OL} = 8 mA		4.5 V			0.36		0.44	
I_I	A or B inputs	$V_I = V_{CC}$ or GND		5.5 V			± 0.1		± 1	μA
I_{CC}		$V_I = V_{CC}$ or GND,	I_O = 0	5.5 V			2		20	μA
C_i		$V_I = V_{CC}$ or GND		5 V		4	10		10	pF

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	OUTPUT CAPACITANCE	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
t_{PLH}	A or B	Y	C_L = 15 pF		6.2	8.8	1	10.5	ns
t_{PHL}					6.2	8.8	1	10.5	
t_{PLH}	A or B	Y	C_L = 50 pF		8.7	12.3	1	14	ns
t_{PHL}					8.7	12.3	1	14	

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	OUTPUT CAPACITANCE	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
t_{PLH}	A or B	Y	C_L = 15 pF		4.3	5.9	1	7	ns
t_{PHL}					4.3	5.9	1	7	
t_{PLH}	A or B	Y	C_L = 50 pF		5.8	7.9	1	9	ns
t_{PHL}					5.8	7.9	1	9	

noise characteristics, V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C (see Note 4)

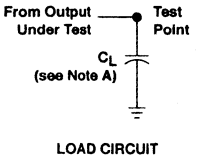
PARAMETER		MIN	TYP	MAX	UNIT
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}			0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}			–0.8	V
$V_{IH(D)}$	High-level dynamic input voltage	3.5			V
$V_{IL(D)}$	Low-level dynamic input voltage			1.5	V

NOTE 4: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

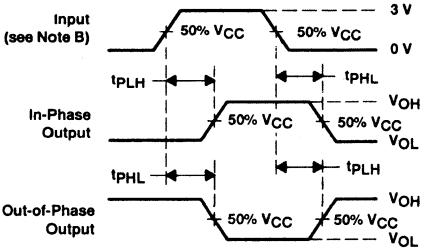
operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	C_L = 50 pF, f = 1 MHz	18	pF

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



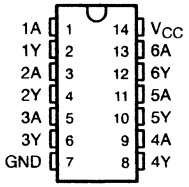
VOLTAGE WAVEFORMS
DELAY TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

- **Operating Range: 2-V to 5.5-V V_{CC}**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **High Latch-Up Immunity Exceeds 300 mA Per JEDEC Standard JESD-17**
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW) Packages, and Standard Plastic (N) DIPs**

D, DB, N, OR PW PACKAGE
(TOP VIEW)



description

The SN74AHC14 contains six independent inverters. The device performs the Boolean function $Y = \overline{A}$.

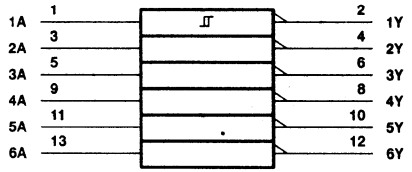
Each circuit functions as an independent inverter, but because of the Schmitt action, the inverters have different input threshold levels for positive- (V_{T+}) and negative-going (V_{T-}) signals.

The SN74AHC14 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each gate)

INPUT A	OUTPUT Y
H	L
L	H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$) ..... − 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ± 20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ± 25 mA
Continuous current through V_{CC} or GND ..... ± 50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2): D package ..... 1.25 W
DB or PW package ..... 0.5 W
N package ..... 1.1 W
Storage temperature range, T_{stg} ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions (see Note 3)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2	5.5	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2 V		−50	μA
		V_{CC} = 3.3 V ± 0.3 V		−4	mA
		V_{CC} = 5 V ± 0.5 V		−8	
I_{OL}	Low-level output current	V_{CC} = 2 V		50	μA
		V_{CC} = 3.3 V ± 0.3 V		4	mA
		V_{CC} = 5 V ± 0.5 V		8	
T_A	Operating free-air temperature		−40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
V_{T+} Positive-going input threshold voltage		3 V			2.2		2.2	V
		4.5 V			3.15		3.15	
		5.5 V			3.85		3.85	
V_{T-} Negative-going input threshold voltage		3 V	0.9			0.9		V
		4.5 V	1.35			1.35		
		5.5 V	1.65			1.65		
ΔV_T Hysteresis ($V_{T+} - V_{T-}$)		3 V	0.3		1.2	0.3	1.2	V
		4.5 V	0.4		1.4	0.4	1.4	
		5.5 V	0.5		1.6	0.5	1.6	
V_{OH}	I_{OH} = – 50 μA	2 V	1.9	2		1.9		V
		3 V	2.9	3		2.9		
		4.5 V	4.4	4.5		4.4		
	I_{OH} = – 4 mA	3 V	2.58			2.48		
	I_{OH} = – 8 mA	4.5 V	3.94			3.8		
V_{OL}	I_{OL} = 50 μA	2 V			0.1		0.1	V
		3 V			0.1		0.1	
		4.5 V			0.1		0.1	
	I_{OL} = 4 mA	3 V			0.36		0.44	
	I_{OL} = 8 mA	4.5 V			0.36		0.44	
I_I	$V_I = V_{CC}$ or GND	5.5 V			± 0.1		± 1	μA
I_{CC}	$V_I = V_{CC}$ or GND, I_O = 0	5.5 V			2		20	μA
C_i	$V_I = V_{CC}$ or GND	5 V		2	10		10	pF

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
t_{PLH}	A	Y	C_L = 15 pF		8.3	12.8	1	15	ns
t_{PHL}					8.3	12.8	1	15	
t_{PLH}	A	Y	C_L = 50 pF		10.8	16.3	1	18.5	ns
t_{PHL}					10.8	16.3	1	18.5	

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
t_{PLH}	A	Y	C_L = 15 pF		5.5	8.6	1	10	ns
t_{PHL}					5.5	8.6	1	10	
t_{PLH}	A	Y	C_L = 50 pF		7	10.6	1	12	ns
t_{PHL}					7	10.6	1	12	

noise characteristics, V_{CC} = 5 V, C_L = 50 pF, $t_r = t_f$ = 3 ns, T_A = 25°C (see Note 4)

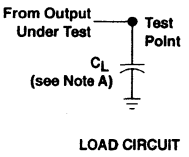
PARAMETER		MIN	TYP	MAX	UNIT
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.8		V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		−0.4		V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}		4.6		V
$V_{IH(D)}$	High-level dynamic input voltage	3.5			V
$V_{IL(D)}$	Low-level dynamic input voltage			1.5	V

NOTE 4: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

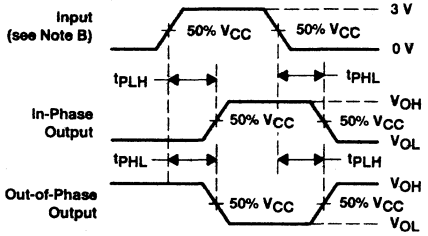
operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	C_L = 50 pF, f = 1 MHz	9	pF

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



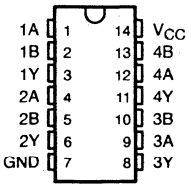
VOLTAGE WAVEFORMS
DELAY TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

- **Operating Range: 2-V to 5.5-V V_{CC}**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **High Latch-Up Immunity Exceeds 300 mA Per JEDEC Standard JESD-17**
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW) Packages, and Standard Plastic (N) DIPs**

D, DB, N, OR PW PACKAGE
(TOP VIEW)



description

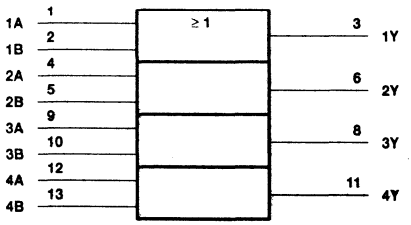
The SN74AHC32 is a quadruple 2-input positive-OR gate. The device performs the Boolean functions $Y = \overline{\overline{A} \bullet \overline{B}}$ or $Y = A + B$ in positive logic.

The SN74AHC32 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each gate)

INPUTS		OUTPUT
A	B	Y
H	X	H
X	H	H
L	L	L

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . −0.5 V to 7 V
Input voltage range, V_I (see Note 1) . . . . . −0.5 V to 7 V
Output voltage range, V_O (see Note 1) . . . . . −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0) . . . . . − 20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) . . . . . ± 20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ± 25 mA
Continuous current through V_{CC} or GND . . . . . ± 50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2): D package . . . . . 1.25 W
DB or PW package . . . . . 0.5 W
N package . . . . . 1.1 W
Storage temperature range, T_{stg} . . . . . −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions (see Note 3)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5		V
		V_{CC} = 3 V	2.1		
		V_{CC} = 5.5 V	3.85		
V_{IL}	Low-level input voltage	V_{CC} = 2 V		0.5	V
		V_{CC} = 3 V		0.9	
		V_{CC} = 5.5 V		1.65	
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2 V		− 50	μA
		V_{CC} = 3.3 V ± 0.3 V		− 4	mA
		V_{CC} = 5 V ± 0.5 V		− 8	
I_{OL}	Low-level output current	V_{CC} = 2 V		50	μA
		V_{CC} = 3.3 V ± 0.3 V		4	mA
		V_{CC} = 5 V ± 0.5 V		8	
$\Delta t/\Delta v$	Input transition rise or fall rate	V_{CC} = 3.3 V ± 0.3 V		100	ns/V
		V_{CC} = 5 V ± 0.5 V		20	
T_A	Operating free-air temperature		− 40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
V_{OH}		I_{OH} = – 50 μA	2 V	1.9	2		1.9		V
			3 V	2.9	3		2.9		
			4.5 V	4.4	4.5		4.4		
		I_{OH} = – 4 mA	3 V	2.58			2.48		
		I_{OH} = – 8 mA	4.5 V	3.94			3.8		
V_{OL}		I_{OL} = 50 μA	2 V			0.1		0.1	V
			3 V			0.1		0.1	
			4.5 V			0.1		0.1	
		I_{OL} = 4 mA	3 V			0.36		0.44	
		I_{OL} = 8 mA	4.5 V			0.36		0.44	
I_I	A or B inputs	V_I = V_{CC} or GND	5.5 V			± 0.1		± 1	μA
I_{CC}		V_I = V_{CC} or GND, I_O = 0	5.5 V			2		20	μA
C_i		V_I = V_{CC} or GND	5 V		2	10		10	pF

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
t_{PLH}	A or B	Y	C_L = 15 pF		5.5	7.9	1	9.5	ns
t_{PHL}					5.5	7.9	1	9.5	
t_{PLH}	A or B	Y	C_L = 50 pF		8	11.4	1	13	ns
t_{PHL}					8	11.4	1	13	

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
t_{PLH}	A or B	Y	C_L = 15 pF		3.8	5.5	1	6.5	ns
t_{PHL}					3.8	5.5	1	6.5	
t_{PLH}	A or B	Y	C_L = 50 pF		5.3	7.5	1	8.5	ns
t_{PHL}					5.3	7.5	1	8.5	

noise characteristics, V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C (see Note 4)

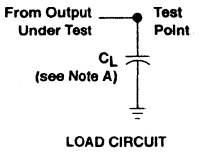
PARAMETER		MIN	TYP	MAX	UNIT
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.3	0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		–0.3	–0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}		4.7		V
$V_{IH(D)}$	High-level dynamic input voltage	3.5			V
$V_{IL(D)}$	Low-level dynamic input voltage			1.5	V

NOTE 4: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

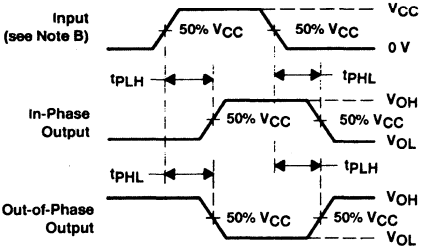
operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	C_L = 50 pF, f = 1 MHz	14	pF

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



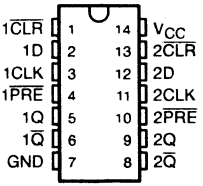
VOLTAGE WAVEFORMS
DELAY TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

- **Operating Range: 2-V to 5.5-V V_{CC}**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW) Packages, and Standard Plastic (N) DIPs**

D, DB, N, OR PW PACKAGE
(TOP VIEW)



description

The SN74AHC74 is a dual positive-edge-triggered D-type flip-flop.

A low level at the preset ($\overline{PRE}$) or clear ($\overline{CLR}$) inputs sets or resets the outputs regardless of the levels of the other inputs. When $\overline{PRE}$ and $\overline{CLR}$ are inactive (high), data at the data (D) input meeting the setup time requirements is transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold-time interval, data at the D input can be changed without affecting the levels at the outputs.

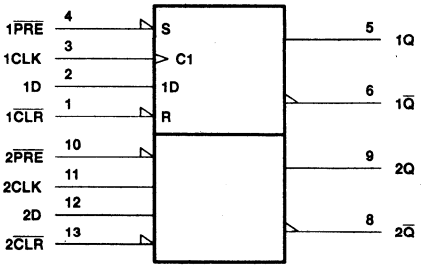
The SN74AHC74 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE

INPUTS				OUTPUTS	
$\overline{PRE}$	$\overline{CLR}$	CLK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H†	H†
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$

† This configuration is nonstable; that is, it does not persist when $\overline{PRE}$ or $\overline{CLR}$ returns to its inactive (high) level.

logic symbol‡



‡ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

PRODUCT PREVIEW

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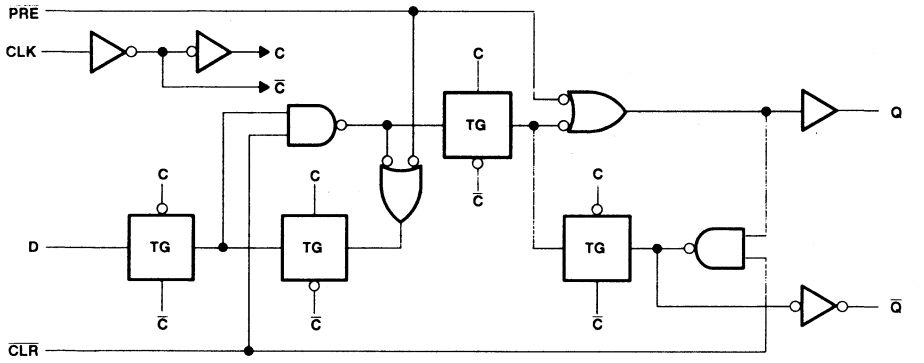
logic diagram, each flip-flop (positive logic)



PRODUCT PREVIEW

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$) ..... − 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ± 20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ± 25 mA
Continuous current through V_{CC} or GND ..... ± 50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2): D package ..... 1.25 W
DB or PW package ..... 0.5 W
N package ..... 1.1 W
Storage temperature range, T_{stg} ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions (see Note 3)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5		V
		V_{CC} = 3 V	2.1		
		V_{CC} = 5.5 V	3.85		
V_{IL}	Low-level input voltage	V_{CC} = 2 V		0.5	V
		V_{CC} = 3 V		0.9	
		V_{CC} = 5.5 V		1.65	
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2 V		– 50	μA
		V_{CC} = 3.3 V ± 0.3 V		– 4	mA
		V_{CC} = 5 V ± 0.5 V		–8	
I_{OL}	Low-level output current	V_{CC} = 2 V		50	μA
		V_{CC} = 3.3 V ± 0.3 V		4	mA
		V_{CC} = 5 V ± 0.5 V		8	
$\Delta t/\Delta v$	Input transition rise or fall rate	V_{CC} = 3.3 V ± 0.3 V		100	ns/V
		V_{CC} = 5 V ± 0.5 V		20	
T_A	Operating free-air temperature		– 40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
V_{OH}		I_{OH} = – 50 μA	2 V	1.9	2		1.9		V
			3 V	2.9	3		2.9		
			4.5 V	4.4	4.5		4.4		
		I_{OH} = – 4 mA	3 V	2.58			2.48		
		I_{OH} = – 8 mA	4.5 V	3.94			3.8		
V_{OL}		I_{OL} = 50 μA	2 V			0.1		0.1	V
			3 V			0.1		0.1	
			4.5 V			0.1		0.1	
		I_{OL} = 4 mA	3 V			0.36		0.44	
		I_{OL} = 8 mA	4.5 V			0.36		0.44	
I_I	Data inputs	V_I = V_{CC} or GND	5.5 V			± 0.1		± 1	μA
	Control inputs					± 0.1		± 1	
I_{CC}		V_I = V_{CC} or GND, I_O = 0	5.5 V			2		20	μA
C_i		V_I = V_{CC} or GND	5 V		4	10		10	pF

PRODUCT PREVIEW

timing requirements over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

			T_A = 25°C		MIN	MAX	UNIT
			MIN	MAX			
t_w	Pulse duration	$\overline{PRE}$ or $\overline{CLR}$ low	6		7		ns
		CLK	6		7		
t_{su}	Setup time before CLK↑	Data	6		7		ns
		$\overline{PRE}$ or $\overline{CLR}$ inactive	6		7		
t_h	Hold time, data after CLK↑		0.5		0.5		ns
t_{rem}	Minimum removal time	$\overline{PRE}$ or $\overline{CLR}$	5		5		ns

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

			T_A = 25°C		MIN	MAX	UNIT
			MIN	MAX			
t_w	Pulse duration	$\overline{PRE}$ or $\overline{CLR}$ low	5		5		ns
		CLK	5		5		
t_{su}	Setup time before CLK↑	Data	5		5		ns
		$\overline{PRE}$ or $\overline{CLR}$ inactive	5		5		
t_h	Hold time, data after CLK↑		0.5		0.5		ns
t_{rem}	Minimum removal time	$\overline{PRE}$ or $\overline{CLR}$	3		3		ns

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
f_{max}			C_L = 15 pF	80	125		70		MHz
f_{max}			C_L = 50 pF	50	75		45		
t_{PLH}	$\overline{PRE}$ or $\overline{CLR}$	Q or $\overline{Q}$	C_L = 15 pF		7.6	12.3	1	14.5	ns
t_{PHL}					7.6	12.3	1	14.5	
t_{PLH}	CLK	Q or $\overline{Q}$			6.7	11.9	1	14	ns
t_{PHL}					6.7	11.9	1	14	
t_{PLH}	$\overline{PRE}$ or $\overline{CLR}$	Q or $\overline{Q}$	C_L = 50 pF		10.1	15.8	1	18	ns
t_{PHL}					10.1	15.8	1	18	
t_{PLH}	CLK	Q or $\overline{Q}$			9.2	15.4	1	17.5	ns
t_{PHL}					9.2	15.4	1	17.5	

PRODUCT PREVIEW

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
f_{max}			C_L = 15 pF	130	170		110		MHz
f_{max}			C_L = 50 pF	90	115		75		
t_{PLH}	$\overline{PRE}$ or $\overline{CLR}$	Q or $\overline{Q}$	C_L = 15 pF		4.8	7.7	1	9	ns
t_{PHL}					4.8	7.7	1	9	
t_{PLH}	CLK	Q or $\overline{Q}$			4.6	7.3	1	8.5	ns
t_{PHL}					4.6	7.3	1	8.5	
t_{PLH}	$\overline{PRE}$ or $\overline{CLR}$	Q or $\overline{Q}$	C_L = 50 pF		6.3	9.7	1	11	ns
t_{PHL}					6.3	9.7	1	11	
t_{PLH}	CLK	Q or Q			6.1	9.3	1	10.5	ns
t_{PHL}					6.1	9.3	1	10.5	

noise characteristics, V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C (see Note 4)

PARAMETER		MIN	TYP	MAX	UNIT
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}			0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}			−0.8	V
$V_{IH(D)}$	High-level dynamic input voltage	3.5			V
$V_{IL(D)}$	Low-level dynamic input voltage			1.5	V

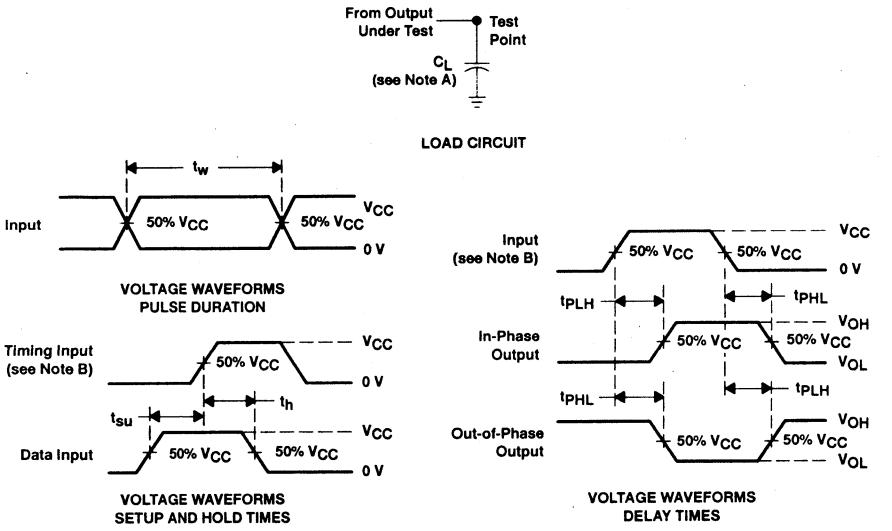
NOTE 4: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_{pd}	Power dissipation capacitance	C_L = 50 pF, f = 1 MHz		25		pF

PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION



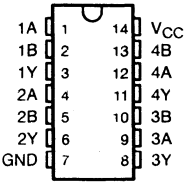
NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PRODUCT PREVIEW

- **Operating Range: 2-V to 5.5-V V_{CC}**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **High Latch-Up Immunity Exceeds 300 mA Per JEDEC Standard JESD-17**
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW) Packages, and Standard Plastic (N) DIPs**

D, DB, N, OR PW PACKAGE
(TOP VIEW)



description

The SN74AHC86 is a quadruple 2-input exclusive-OR gate. The device performs the Boolean functions $Y = A \oplus B$ or $Y = \overline{A}B + A\overline{B}$ in positive logic.

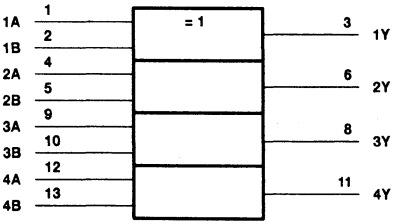
A common application is as a true/complement element. If one of the inputs is low, the other input is reproduced in true form at the output. If one of the inputs is high, the signal on the other input is reproduced inverted at the output.

The SN74AHC86 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each gate)

INPUTS		OUTPUT
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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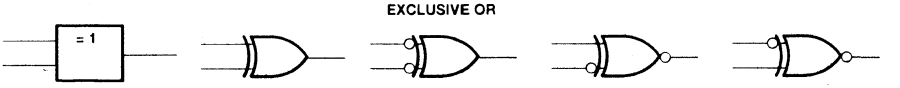
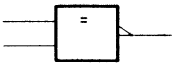
exclusive-OR logic

An exclusive-OR gate has many applications, some of which can be represented better by alternative logic symbols.



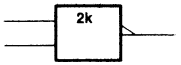
These are five equivalent exclusive-OR symbols valid for an SN74AHC86 gate in positive logic; negation may be shown at any two ports.

LOGIC-IDENTITY ELEMENT



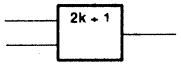
The output is active (low) if all inputs stand at the same logic level (i.e., A = B).

EVEN-PARITY ELEMENT



The output is active (low) if an even number of inputs (i.e., 0 or 2) are active.

ODD-PARITY ELEMENT



The output is active (high) if an odd number of inputs (i.e., only 1 of the 2) are active.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Output voltage range, V_O (see Note 1)	–0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$)	–20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC})	±25 mA
Continuous current through V_{CC} or GND	±50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2): D package	1.25 W
DB or PW package	0.5 W
N package	1.1 W
Storage temperature range, T_{stg}	–65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions (see Note 3)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5		V
		V_{CC} = 3 V	2.1		
		V_{CC} = 5.5 V	3.85		
V_{IL}	Low-level input voltage	V_{CC} = 2 V		0.5	V
		V_{CC} = 3 V		0.9	
		V_{CC} = 5.5 V		1.65	
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2 V		–50	μA
		V_{CC} = 3.3 V ± 0.3 V		–4	mA
		V_{CC} = 5 V ± 0.5 V		–8	
I_{OL}	Low-level output current	V_{CC} = 2 V		50	μA
		V_{CC} = 3.3 V ± 0.3 V		4	mA
		V_{CC} = 5 V ± 0.5 V		8	
$\Delta t/\Delta v$	Input transition rise or fall rate	V_{CC} = 3.3 V ± 0.3 V		100	ns/V
		V_{CC} = 5 V ± 0.5 V		20	
T_A	Operating free-air temperature		–40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
V_{OH}		I_{OH} = –50 μA	2 V	1.9	2		1.9		V
			3 V	2.9	3		2.9		
			4.5 V	4.4	4.5		4.4		
		I_{OH} = –4 mA	3 V	2.58			2.48		
		I_{OH} = –8 mA	4.5 V	3.94			3.8		
V_{OL}		I_{OL} = 50 μA	2 V			0.1		0.1	V
			3 V			0.1		0.1	
			4.5 V			0.1		0.1	
		I_{OL} = 4 mA	3 V			0.36		0.44	
		I_{OL} = 8 mA	4.5 V			0.36		0.44	
I_I	A or B inputs	V_I = V_{CC} or GND	5.5 V			± 0.1		± 1	μA
I_{CC}		V_I = V_{CC} or GND, I_O = 0	5.5 V			2		20	μA
C_i		V_I = V_{CC} or GND	5 V		4	10		10	pF

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	OUTPUT CAPACITANCE	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
t_{PLH}	A or B	Y	C_L = 15 pF		7	11	1	13	ns
t_{PHL}					7	11	1	13	
t_{PLH}	A or B	Y	C_L = 50 pF		9.5	14.5	1	16.5	ns
t_{PHL}					9.5	14.5	1	16.5	

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	OUTPUT CAPACITANCE	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
t_{PLH}	A or B	Y	C_L = 15 pF		4.8	6.8	1	8	ns
t_{PHL}					4.8	6.8	1	8	
t_{PLH}	A or B	Y	C_L = 50 pF		6.3	8.8	1	10	ns
t_{PHL}					6.3	8.8	1	10	

noise characteristics, V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C (see Note 4)

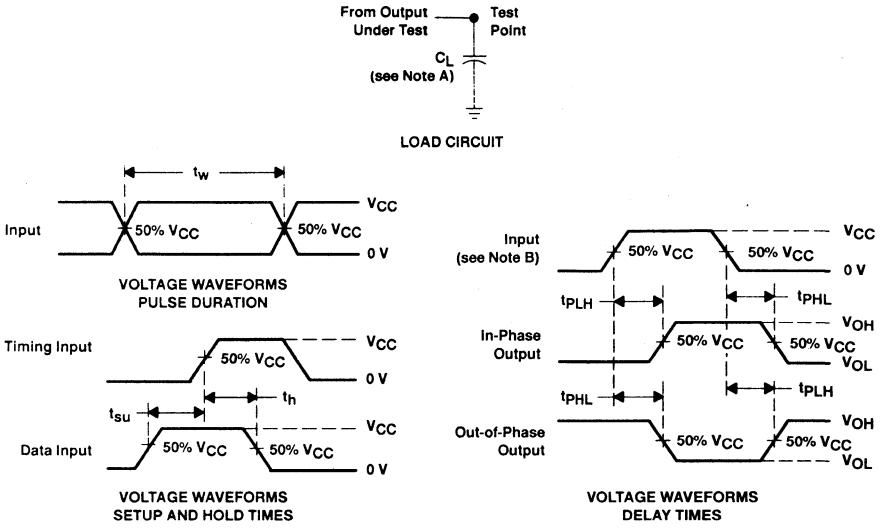
PARAMETER		MIN	TYP	MAX	UNIT
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.3	0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		–0.3	–0.8	V
$V_{IH(D)}$	High-level dynamic input voltage	3.5			V
$V_{IL(D)}$	Low-level dynamic input voltage			1.5	V

NOTE 4: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	C_L = 50 pF, f = 1 MHz	18	pF

PARAMETER MEASUREMENT INFORMATION

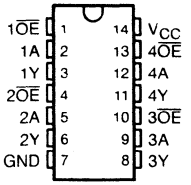


NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

- **Operating Range: 2-V to 5.5-V V_{CC}**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW) Packages, and Standard Plastic (N) DIPs**

D, DB, N, OR PW PACKAGE
(TOP VIEW)



description

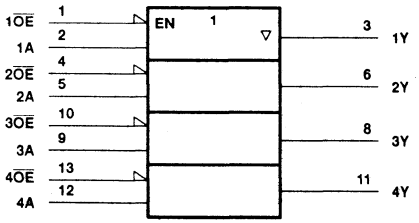
The SN74AHC125 quadruple bus buffer gate features independent line drivers with 3-state outputs. Each output is disabled when the associated output-enable ($\overline{OE}$) input is high. When $\overline{OE}$ is low, the respective gate passes the data from the A input to its Y output.

The SN74AHC125 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each buffer)

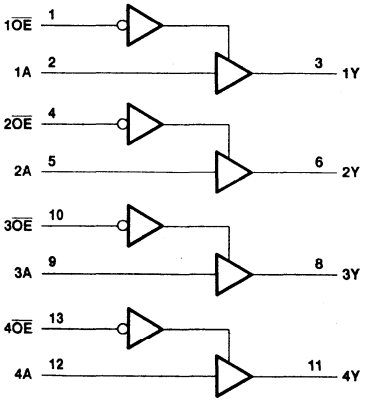
INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	H
L	L	L
H	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



PRODUCT PREVIEW

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$) ..... − 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ± 20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ± 25 mA
Continuous current through V_{CC} or GND ..... ± 50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2): D package ..... 1.25 W
DB or PW package ..... 0.5 W
N package ..... 1.1 W
Storage temperature range, T_{stg} ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions (see Note 3)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5		V
		V_{CC} = 3 V	2.1		
		V_{CC} = 5.5 V	3.85		
V_{IL}	Low-level input voltage	V_{CC} = 2 V		0.5	V
		V_{CC} = 3 V		0.9	
		V_{CC} = 5.5 V		1.65	
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2 V		− 50	μA
		V_{CC} = 3.3 V ± 0.3 V		− 4	mA
		V_{CC} = 5 V ± 0.5 V		− 8	
I_{OL}	Low-level output current	V_{CC} = 2 V		50	μA
		V_{CC} = 3.3 V ± 0.3 V		4	mA
		V_{CC} = 5 V ± 0.5 V		8	
$\Delta t/\Delta v$	Input transition rise or fall rate	Vcc = 3.3 V ± 0.3 V		100	ns/V
		Vcc = 5 V ± 0.5 V		20	
T_A	Operating free-air temperature		− 40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
V_{OH}		I_{OH} = – 50 μA	2 V	1.9	2		1.9		V
			3 V	2.9	3		2.9		
			4.5 V	4.4	4.5		4.4		
		I_{OH} = – 4 mA	3 V	2.58			2.48		
		I_{OH} = – 8 mA	4.5 V	3.94			3.8		
V_{OL}		I_{OL} = 50 μA	2 V			0.1		0.1	V
			3 V			0.1		0.1	
			4.5 V			0.1		0.1	
		I_{OL} = 4 mA	3 V			0.36		0.44	
		I_{OL} = 8 mA	4.5 V			0.36		0.44	
I_I	A or $\overline{OE}$ inputs	V_I = V_{CC} or GND	5.5 V			± 0.1		± 1	μA
I_{OZ}		V_I = V_{CC} or GND	5.5 V			± 0.25		± 2.5	μA
I_{CC}		V_I = V_{CC} or GND, I_O = 0	5.5 V			2		20	μA
C_i		V_I = V_{CC} or GND	5 V		4	10		10	pF

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
t_{PLH}	A	Y	C_L = 15 pF						ns
t_{PHL}									
t_{PZH}	$\overline{OE}$	Y							ns
t_{PZL}									
t_{PHZ}	$\overline{OE}$	Y							ns
t_{PLZ}									
t_{PLH}	A	Y	C_L = 50 pF						ns
t_{PHL}									
t_{PZH}	$\overline{OE}$	Y							ns
t_{PZL}									
t_{PHZ}	$\overline{OE}$	Y							ns
t_{PLZ}									

PRODUCT PREVIEW

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
t_{PLH}	A	Y	C_L = 15 pF						ns
t_{PHL}									
t_{PZH}	OE	Y							ns
t_{PZL}									
t_{PHZ}	OE	Y							ns
t_{PLZ}									
t_{PLH}	A	Y	C_L = 50 pF						ns
t_{PHL}									
t_{PZH}	$\overline{OE}$	Y							ns
t_{PZL}									
t_{PHZ}	$\overline{OE}$	Y							ns
t_{PLZ}									

output-skew characteristics, C_L = 50 pF (see Note 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
$t_{sk(o)}$	A	Y	3.3 V ± 0.3 V			1.5		1.5	ns
			5 V ± 0.5 V			1		1	

NOTE 4: Characteristics are determined during product characterization and ensured by design.

noise characteristics V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C (see Note 5)

PARAMETER		MIN	TYP	MAX	UNIT
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}			0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}			−0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}				V
$V_{IH(D)}$	High-level dynamic input voltage	3.5			V
$V_{IL(D)}$	Low-level dynamic input voltage			1.5	V

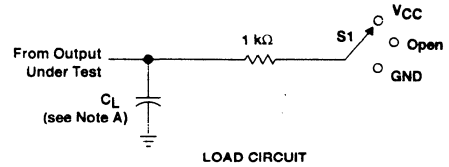
NOTE 5: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
C_{pd}	Power dissipation capacitance	C_L = 50 pF,	f = 1 MHz				pF

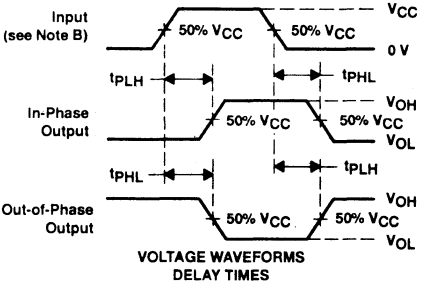
PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

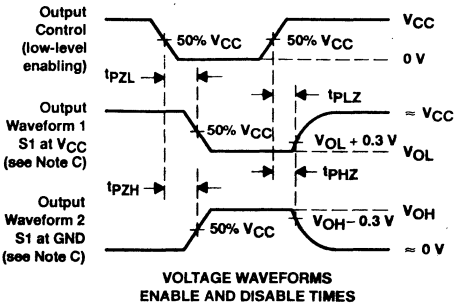


LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND



VOLTAGE WAVEFORMS
DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

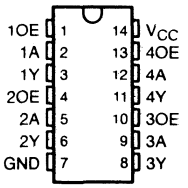
NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PRODUCT PREVIEW

- **Operating Range: 2-V to 5.5-V V_{CC}**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW) Packages, and Standard Plastic (N) DIPs**

D, DB, N, OR PW PACKAGE
(TOP VIEW)



description

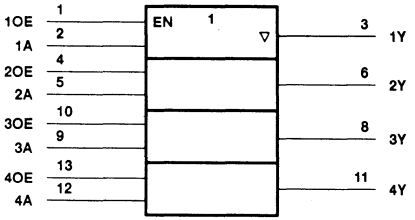
The SN74AHC126 quadruple bus buffer gate features independent line drivers with 3-state outputs. Each output is disabled when the associated output-enable (OE) input is low. When OE is high, the respective gate passes the data from the A input to its Y output.

The SN74AHC126 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each buffer)

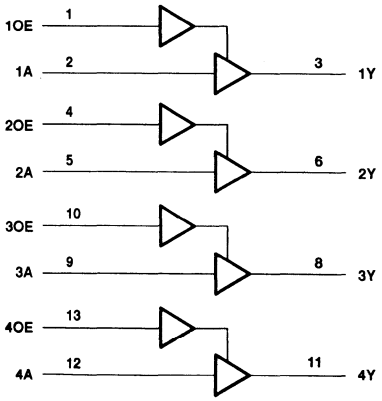
INPUTS		OUTPUT
OE	A	Y
H	H	H
H	L	L
L	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0) ..... − 20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ± 20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ± 25 mA
Continuous current through V_{CC} or GND ..... ± 50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2): D package ..... 1.25 W
DB or PW package ..... 0.5 W
N package ..... 1.1 W
Storage temperature range, T_{stg} ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

PRODUCT PREVIEW

recommended operating conditions (see Note 3)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5		V
		V_{CC} = 3 V	2.1		
		V_{CC} = 5.5 V	3.85		
V_{IL}	Low-level input voltage	V_{CC} = 2 V		0.5	V
		V_{CC} = 3 V		0.9	
		V_{CC} = 5.5 V		1.65	
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2 V		− 50	μA
		V_{CC} = 3.3 V ± 0.3 V		− 4	mA
		V_{CC} = 5 V ± 0.5 V		− 8	
I_{OL}	Low-level output current	V_{CC} = 2 V		50	μA
		V_{CC} = 3.3 V ± 0.3 V		4	mA
		V_{CC} = 5 V ± 0.5 V		8	
$\Delta t/\Delta v$	Input transition rise or fall rate	Vcc = 3.3 V ± 0.3 V		100	ns/V
		Vcc = 5 V ± 0.5 V		20	
T_A	Operating free-air temperature		− 40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
V_{OH}		I_{OH} = – 50 μA	2 V	1.9	2		1.9		V
			3 V	2.9	3		2.9		
			4.5 V	4.4	4.5		4.4		
		I_{OH} = – 4 mA	3 V	2.58			2.48		
		I_{OH} = – 8 mA	4.5 V	3.94			3.8		
V_{OL}		I_{OL} = 50 μA	2 V			0.1		0.1	V
			3 V			0.1		0.1	
			4.5 V			0.1		0.1	
		I_{OL} = 4 mA	3 V			0.36		0.44	
		I_{OL} = 8 mA	4.5 V			0.36		0.44	
I_I	A or OE inputs	V_I = V_{CC} or GND	5.5 V			± 0.1		± 1	μA
I_{OZ}		V_I = V_{CC} or GND	5.5 V			± 0.25		± 2.5	μA
I_{CC}		V_I = V_{CC} or GND, I_O = 0	5.5 V			2		20	μA
C_i		V_I = V_{CC} or GND	5 V		4	10		10	pF

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
t_{PLH}	A	Y	C_L = 15 pF						ns
t_{PHL}									
t_{PZH}	OE	Y							ns
t_{PZL}									
t_{PHZ}	OE	Y							ns
t_{PLZ}									
t_{PLH}	A	Y	C_L = 50 pF						ns
t_{PHL}									
t_{PZH}	OE	Y							ns
t_{PZL}									
t_{PHZ}	OE	Y							ns
t_{PLZ}									

PRODUCT PREVIEW

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
t_{PLH}	A	Y	C_L = 15 pF						ns
t_{PHL}									
t_{PZH}	OE	Y							ns
t_{PZL}									
t_{PHZ}	OE	Y							ns
t_{PLZ}									
t_{PLH}	A	Y	C_L = 50 pF						ns
t_{PHL}									
t_{PZH}	OE	Y							ns
t_{PZL}									
t_{PHZ}	OE	Y							ns
t_{PLZ}									

output-skew characteristics, C_L = 50 pF (see Note 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
$t_{sk(o)}$	A	Y	3.3 V ± 0.3 V			1.5		1.5	ns
			5 V ± 0.5 V			1		1	

NOTE 4: Characteristics are determined during product characterization and ensured by design.

noise characteristics V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C (see Note 5)

	PARAMETER	MIN	TYP	MAX	UNIT
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}			0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}			−0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}				V
$V_{IH(D)}$	High-level dynamic input voltage	3.5			V
$V_{IL(D)}$	Low-level dynamic input voltage			1.5	V

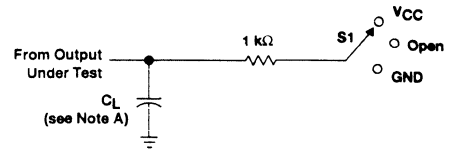
NOTE 5: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

operating characteristics, V_{CC} = 5 V, T_A = 25°C

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_{pd}	Power dissipation capacitance	C_L = 50 pF, f = 1 MHz				pF

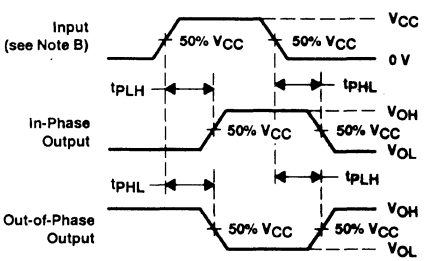
PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

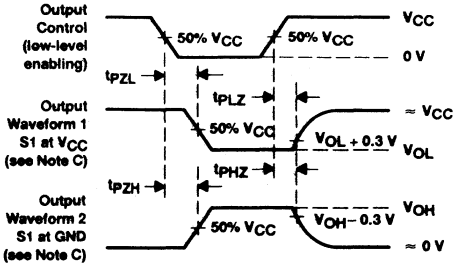


LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND



VOLTAGE WAVEFORMS
DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one input transition per measurement.

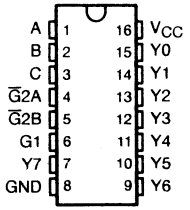
Figure 1. Load Circuit and Voltage Waveforms

PRODUCT PREVIEW

SCLS258A – DECEMBER 1995 – REVISED JANUARY 1996

- **Operating Range: 2-V to 5.5-V V_{CC}**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **Designed Specifically for High-Speed Memory Decoders and Data Transmission Systems**
- **Incorporates Three Enable Inputs to Simplify Cascading and/or Data Reception**
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW) Packages, and Standard Plastic (N) DIPs**

D, DB, N, OR PW PACKAGE
(TOP VIEW)



description

The SN74AHC138 decoder/demultiplexer is designed for high-performance memory-decoding or data-routing applications requiring very short propagation-delay times. In high-performance memory systems, this decoder can be used to minimize the effects of system decoding. When employed with high-speed memories utilizing a fast enable circuit, the delay times of this decoder and the enable time of the memory are usually less than the typical access time of the memory. This means that the effective system delay introduced by the decoder is negligible.

The conditions at the binary-select inputs and the three enable inputs select one of eight input lines. Two active-low and one active-high enable inputs reduce the need for external gates or inverters when expanding. A 24-line decoder can be implemented without external inverters and a 32-line decoder requires only one inverter. An enable input can be used as a data input for demultiplexing applications.

The SN74AHC138 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE

ENABLE INPUTS			SELECT INPUTS			OUTPUTS							
G1	$\overline{G2A}$	$\overline{G2B}$	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	L	H	H	H	H	H	L	H	H	H	H
H	L	L	H	L	L	H	H	H	H	L	H	H	H
H	L	L	H	L	H	H	H	H	H	H	L	H	H
H	L	L	H	H	L	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L

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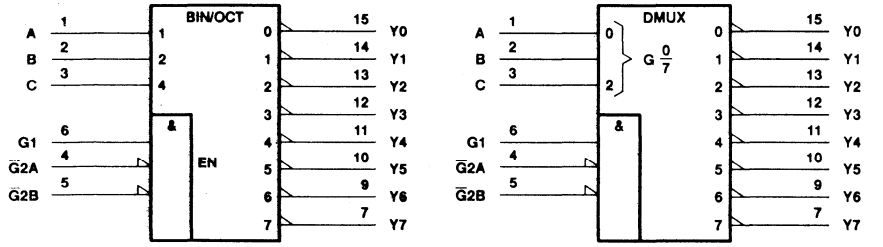
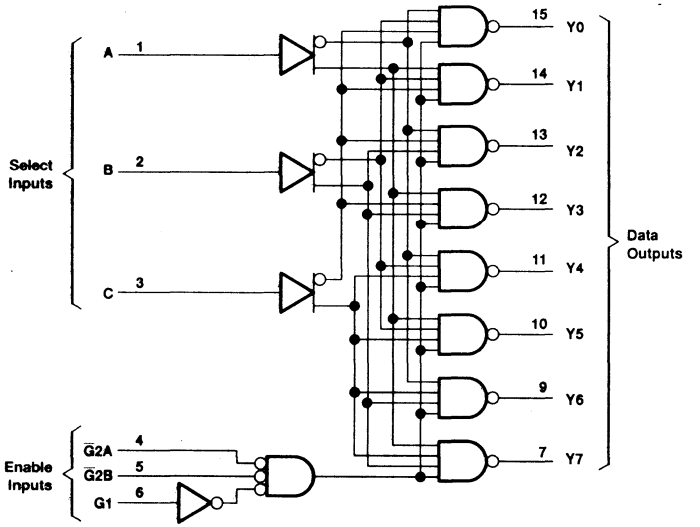
logic symbols (alternatives)†



† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



PRODUCT PREVIEW

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0) ..... − 20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ± 20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ± 25 mA
Continuous current through V_{CC} or GND ..... ± 75 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2): D package ..... 1.3 W
DB package ..... 0.55 W
N package ..... 1.1 W
PW package ..... 0.5 W
Storage temperature range, T_{stg} ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions (see Note 3)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5		V
		V_{CC} = 3 V	2.1		
		V_{CC} = 5.5 V	3.85		
V_{IL}	Low-level input voltage	V_{CC} = 2 V		0.5	V
		V_{CC} = 3 V		0.9	
		V_{CC} = 5.5 V		1.65	
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2 V		− 50	μA
		V_{CC} = 3.3 V ± 0.3 V		− 4	mA
		V_{CC} = 5 V ± 0.5 V		− 8	
I_{OL}	Low-level output current	V_{CC} = 2 V		50	μA
		V_{CC} = 3.3 V ± 0.3 V		4	mA
		V_{CC} = 5 V ± 0.5 V		8	
$\Delta t/\Delta v$	Input transition rise or fall rate	Vcc = 3.3 V ± 0.3 V		100	ns/V
		Vcc = 5 V ± 0.5 V		20	
T_A	Operating free-air temperature		− 40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
V_{OH}	I_{OH} = – 50 μA	2 V	1.9	2		1.9		V
		3 V	2.9	3		2.9		
		4.5 V	4.4	4.5		4.4		
	I_{OH} = – 4 mA	3 V	2.58			2.48		
	I_{OH} = – 8 mA	4.5 V	3.94			3.8		
V_{OL}	I_{OL} = 50 μA	2 V			0.1		0.1	V
		3 V			0.1		0.1	
		4.5 V			0.1		0.1	
	I_{OL} = 4 mA	3 V			0.36		0.44	
	I_{OL} = 8 mA	4.5 V			0.36		0.44	
I_I	V_I = V_{CC} or GND	5.5 V			± 0.1		± 1	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			4		40	μA
C_i	V_I = V_{CC} or GND	5 V		4	10		10	pF

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
t_{PLH}	A, B, C	Any Y	C_L = 15 pF		8.2	11.4	1	13	ns
t_{PHL}					8.2	11.4	1	13	
t_{PLH}	G1	Any Y			8.1	12.8	1	15	ns
t_{PHL}					8.1	12.8	1	15	
t_{PLH}	$\overline{G}$2A, $\overline{G}$2B	Any Y			8.2	11.4	1	13.5	ns
t_{PHL}					8.2	11.4	1	13.5	
t_{PLH}	A, B, C	Any Y	C_L = 50 pF		10	15.8	1	18	ns
t_{PHL}					10	15.8	1	18	
t_{PLH}	G1	Any Y			10.6	16.3	1	18.5	ns
t_{PHL}					10.6	16.3	1	18.5	
t_{PLH}	$\overline{G}$2A, $\overline{G}$2B	Any Y			10.7	14.9	1	17	ns
t_{PHL}					10.7	14.9	1	17	

PRODUCT PREVIEW

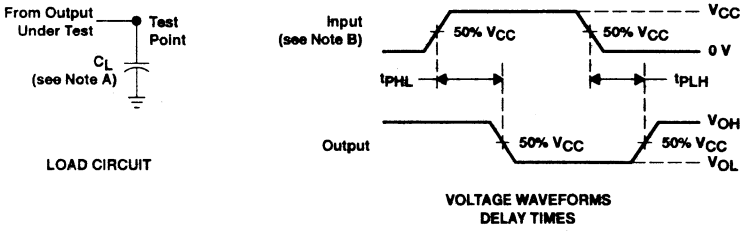
switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
t_{PLH}	A, B, C	Any Y	C_L = 15 pF		5.7	8.1	1	9.5	ns
t_{PHL}					5.7	8.1	1	9.5	
t_{PLH}	G1	Any Y			5.6	8.1	1	9.5	ns
t_{PHL}					5.6	8.1	1	9.5	
t_{PLH}	$\overline{G}$2A, $\overline{G}$2B	Any Y			5.8	8.1	1	9.5	ns
t_{PHL}					5.8	8.1	1	9.5	
t_{PLH}	A, B, C	Any Y	C_L = 50 pF		7.2	10.1	1	11.5	ns
t_{PHL}					7.2	10.1	1	11.5	
t_{PLH}	G1	Any Y			7.1	10.1	1	11.5	ns
t_{PHL}					7.1	10.1	1	11.5	
t_{PLH}	$\overline{G}$2A, $\overline{G}$2B	Any Y			7.3	10.1	1	11.5	ns
t_{PHL}					7.3	10.1	1	11.5	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per gate	C_L = 50 pF, f = 1 MHz	34	pF

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PRODUCT PREVIEW

APPLICATION INFORMATION

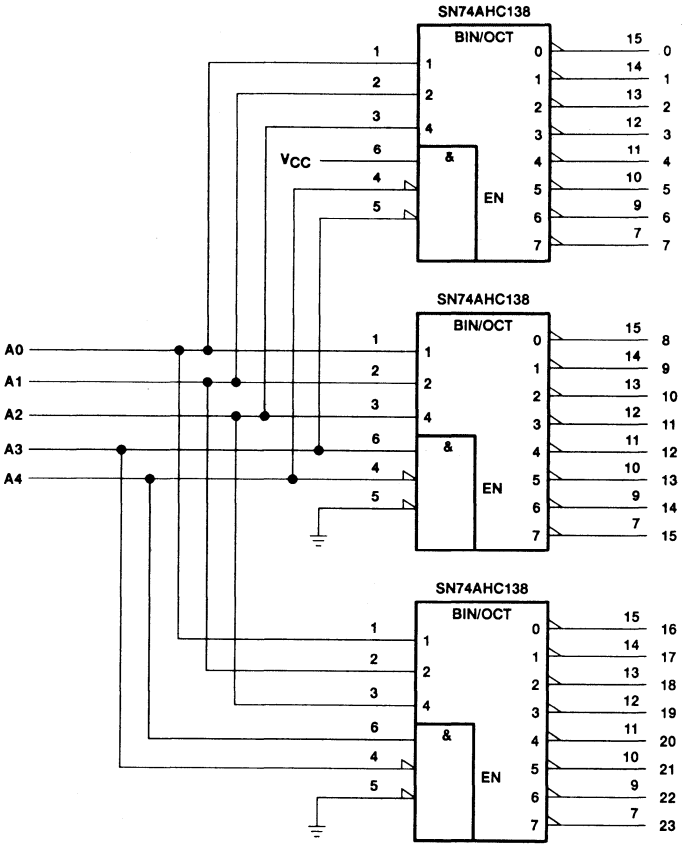


Figure 2. 24-Bit Decoding Scheme

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APPLICATION INFORMATION

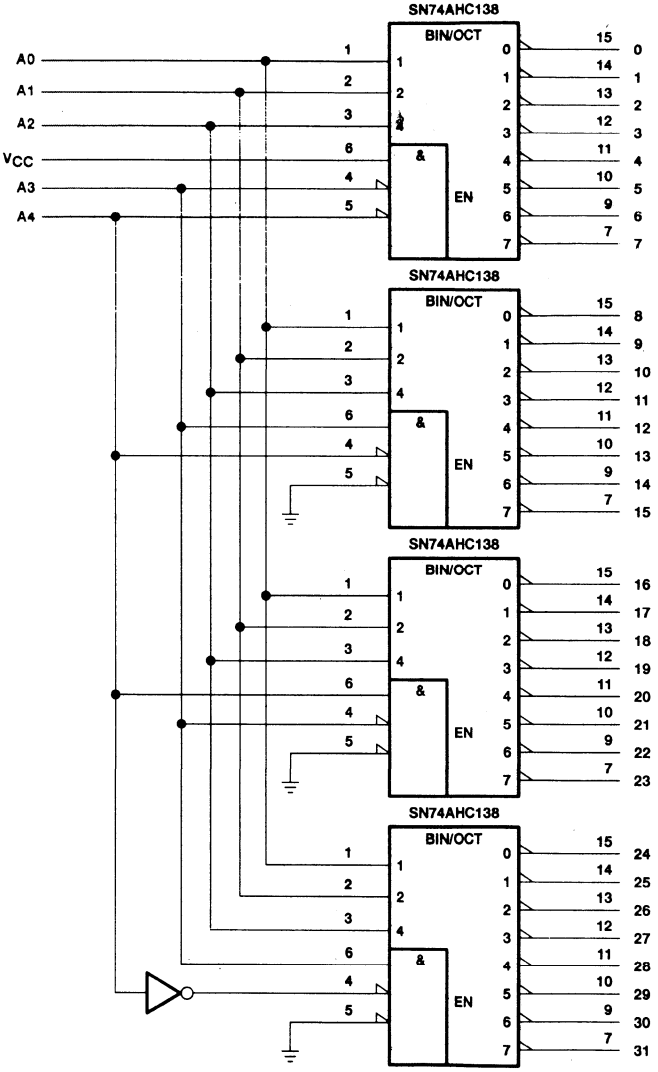


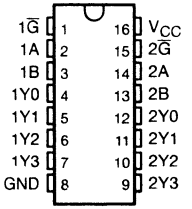
Figure 3. 32-Bit Decoding Scheme

PRODUCT PREVIEW

SCLS259B – DECEMBER 1995 – REVISED FEBRUARY 1996

- Operating Range: 2-V to 5.5-V V_{CC}
- *EPIC*™ (Enhanced-Performance Implanted CMOS) Submicron Process
- Designed Specifically for High-Speed Memory Decoders and Data Transmission Systems
- Incorporates Two Enable Inputs to Simplify Cascading and/or Data Reception
- Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW) Packages, and Standard Plastic (N) DIPs

D, DB, N, OR PW PACKAGE
(TOP VIEW)



description

The SN74AHC139 is a dual 2-line to 4-line decoder/demultiplexer designed for 2-V to 5.5-V V_{CC} operation. This device is designed to be used in high-performance memory-decoding or data-routing applications requiring very short propagation delay times. In high-performance memory systems, this decoder can be used to minimize the effects of system decoding. When used with high-speed memories utilizing a fast enable circuit, the delay times of this decoder and the enable time of the memory are usually less than the typical access time of the memory. This means that the effective system delay introduced by the decoder is negligible.

The active-low enable ($\overline{G}$) input can be used as a data line in demultiplexing applications. These decoders/demultiplexers feature fully buffered inputs, each of which represents only one normalized load to its driving circuit.

The SN74AHC139 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE

INPUTS			OUTPUTS			
$\overline{G}$	SELECT					
	B	A	Y0	Y1	Y2	Y3
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L

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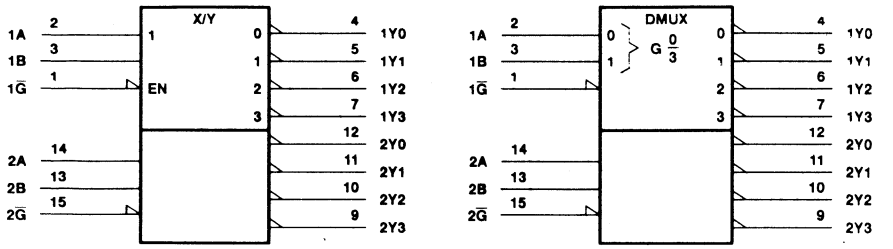
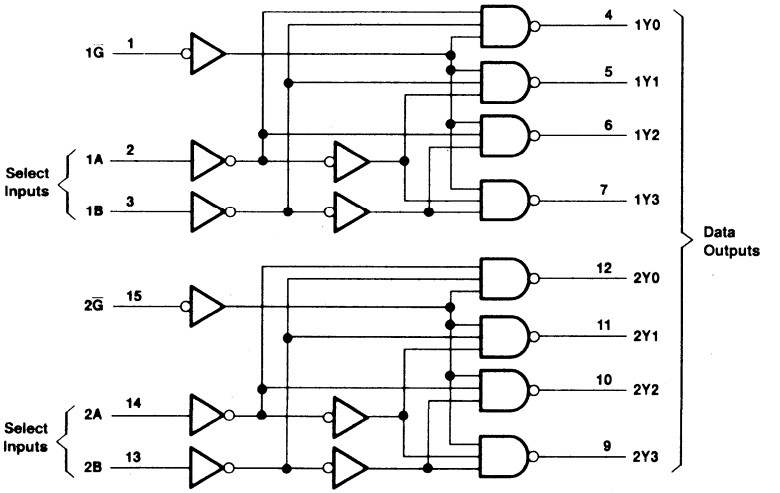
logic symbols (alternatives)†



† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



PRODUCT PREVIEW

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... –0.5 V to 7 V
Output voltage range, V_O (see Note 1) ..... –0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0) ..... –20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±25 mA
Continuous current through V_{CC} or GND ..... ±75 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2): D package ..... 1.3 W
DB package ..... 0.55 W
N package ..... 1.1 W
PW package ..... 0.5 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions (see Note 3)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5		V
		V_{CC} = 3 V	2.1		
		V_{CC} = 5.5 V	3.85		
V_{IL}	Low-level input voltage	V_{CC} = 2 V		0.5	V
		V_{CC} = 3 V		0.9	
		V_{CC} = 5.5 V		1.65	
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2 V		–50	µA
		V_{CC} = 3.3 V ± 0.3 V		–4	mA
		V_{CC} = 5 V ± 0.5 V		–8	
I_{OL}	Low-level output current	V_{CC} = 2 V		50	µA
		V_{CC} = 3.3 V ± 0.3 V		4	mA
		V_{CC} = 5 V ± 0.5 V		8	
$\Delta t/\Delta v$	Input transition rise or fall rate	V_{CC} = 3.3 V ± 0.3 V		100	ns/V
		V_{CC} = 5 V ± 0.5 V		20	
T_A	Operating free-air temperature		–40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
V_{OH}	I_{OH} = –50 μA		2 V	1.9	2		1.9		V
			3 V	2.9	3		2.9		
			4.5 V	4.4	4.5		4.4		
	I_{OH} = –4 mA		3 V	2.58			2.48		
	I_{OH} = –8 mA		4.5 V	3.94			3.8		
V_{OL}	I_{OL} = 50 μA		2 V			0.1		0.1	V
			3 V			0.1		0.1	
			4.5 V			0.1		0.1	
	I_{OL} = 4 mA		3 V			0.36		0.44	
	I_{OL} = 8 mA		4.5 V			0.36		0.44	
I_I	V_I = V_{CC} or GND		5.5 V			±0.1		±1	μA
I_{CC}	V_I = V_{CC} or GND,	I_O = 0	5.5 V			4		40	μA
C_i	V_I = V_{CC} or GND		5 V		4	10		10	pF

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	OUTPUT CAPACITANCE	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
t_{PLH}	A or B	Y	C_L = 15 pF		7.2	11	1	13	ns
t_{PHL}					7.2	11	1	13	
t_{PLH}	$\overline{G}$	Y	C_L = 15 pF		6.4	9.2	1	11	ns
t_{PHL}					6.4	9.2	1	11	
t_{PLH}	A or B	Y	C_L = 50 pF		9.7	14.5	1	16.5	ns
t_{PHL}					9.7	14.5	1	16.5	
t_{PLH}	$\overline{G}$	Y	C_L = 50 pF		8.9	12.7	1	14.5	ns
t_{PHL}					8.9	12.7	1	14.5	

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

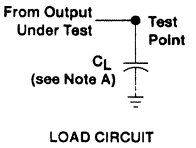
PARAMETER	FROM (INPUT)	TO (OUTPUT)	OUTPUT CAPACITANCE	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
t_{PLH}	A or B	Y	C_L = 15 pF		5	7.2	1	8.5	ns
t_{PHL}					5	7.2	1	8.5	
t_{PLH}	$\overline{G}$	Y	C_L = 15 pF		4.4	6.3	1	7.5	ns
t_{PHL}					4.4	6.3	1	7.5	
t_{PLH}	A or B	Y	C_L = 50 pF		6.5	9.2	1	10.5	ns
t_{PHL}					6.5	9.2	1	10.5	
t_{PLH}	$\overline{G}$	Y	C_L = 50 pF		5.9	8.3	1	9.5	ns
t_{PHL}					5.9	8.3	1	9.5	

PRODUCT PREVIEW

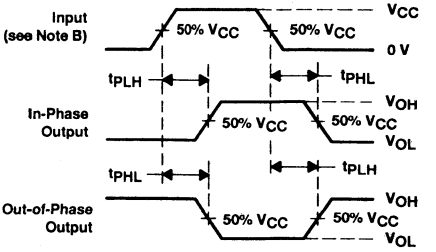
operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per gate	C_L = 50 pF, f = 1 MHz	26	pF

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



VOLTAGE WAVEFORMS
DELAY TIMES

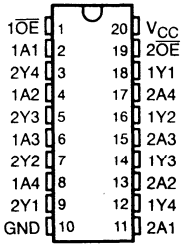
NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PRODUCT PREVIEW

- **Operating Range: 2-V to 5.5-V V_{CC}**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **High Latch-Up Immunity Exceeds 300 mA Per JEDEC Standard JESD-17**
- **Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW) Packages, and Standard Plastic (N) DIPs**

DB, DW, N, OR PW PACKAGE
(TOP VIEW)



description

This octal buffer/driver is designed specifically to improve both the performance and density of 3-state memory-address drivers, clock drivers, and bus-oriented receivers and transmitters.

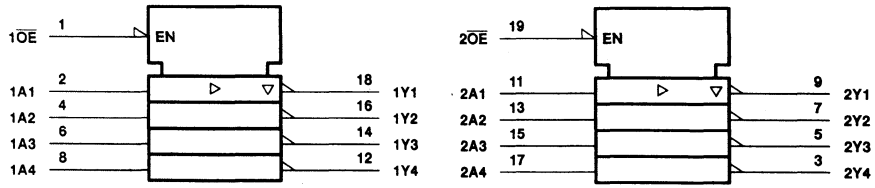
The SN74AHC240 is organized as two 4-bit buffers/line drivers with separate output-enable ($\overline{OE}$) inputs. When $\overline{OE}$ is low, the device passes data from the A inputs to the Y outputs. When $\overline{OE}$ is high, the outputs are in the high-impedance state.

The SN74AHC240 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each buffer)

INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	L
L	L	H
H	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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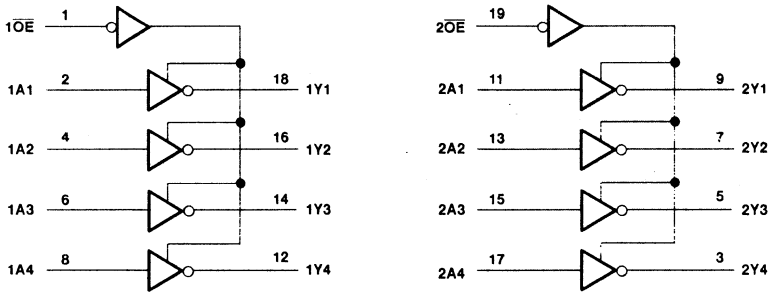
logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... –0.5 V to 7 V
Output voltage range, V_O (see Note 1) ..... –0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) ..... –20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±25 mA
Continuous current through V_{CC} or GND ..... ±75 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2): DB package ..... 0.6 W
DW package ..... 1.6 W
N package ..... 1.3 W
PW package ..... 0.7 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions (see Note 3)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5		V
		V_{CC} = 3 V	2.1		
		V_{CC} = 5.5 V	3.85		
V_{IL}	Low-level input voltage	V_{CC} = 2 V		0.5	V
		V_{CC} = 3 V		0.9	
		V_{CC} = 5.5 V		1.65	
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2 V		–50	μA
		V_{CC} = 3.3 V ± 0.3 V		–4	mA
		V_{CC} = 5 V ± 0.5 V		–8	
I_{OL}	Low-level output current	V_{CC} = 2 V		50	μA
		V_{CC} = 3.3 V ± 0.3 V		4	mA
		V_{CC} = 5 V ± 0.5 V		8	
$\Delta t/\Delta v$	Input transition rise or fall rate	V_{CC} = 3.3 V ± 0.3 V		100	ns/V
		V_{CC} = 5 V ± 0.5 V		20	
T_A	Operating free-air temperature		–40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
V_{OH}		I_{OH} = –50 μA	2 V	1.9	2		1.9		V
			3 V	2.9	3		2.9		
			4.5 V	4.4	4.5		4.4		
		I_{OH} = –4 mA	3 V	2.58			2.48		
		I_{OH} = –8 mA	4.5 V	3.94			3.8		
V_{OL}		I_{OL} = 50 μA	2 V			0.1		0.1	V
			3 V			0.1		0.1	
			4.5 V			0.1		0.1	
		I_{OL} = 4 mA	3 V			0.36		0.44	
		I_{OL} = 8 mA	4.5 V			0.36		0.44	
I_I	Data inputs	V_I = V_{CC} or GND	5.5 V			±0.1		±1	μA
	Control inputs					±0.1		±1	
I_{OZ}†		V_O = V_{CC} or GND, V_I ($\overline{OE}$) = V_{IL} or V_{IH}	5.5 V			±0.25		±2.5	μA
I_{CC}		V_I = V_{CC} or GND, I_O = 0	5.5 V			4		40	μA
C_i		V_I = V_{CC} or GND	5 V		2.5	10		10	pF
C_o		V_O = V_{CC} or GND	5 V		3.5				pF

† The parameter I_{OZ} includes the input leakage current.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	OUTPUT CAPACITANCE	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
t_{PLH}	A	Y	C_L = 15 pF		5.3	7.5	1	9	ns
t_{PHL}					5.3	7.5	1	9	
t_{PZH}	$\overline{OE}$	Y	C_L = 15 pF		6.6	10.6	1	12.5	ns
t_{PZL}					6.6	10.6	1	12.5	
t_{PHZ}	$\overline{OE}$	Y	C_L = 15 pF		7.8	11.5	1	12.5	ns
t_{PLZ}					7.8	11.5	1	12.5	
t_{PLH}	A	Y	C_L = 50 pF		7.8	11	1	12.5	ns
t_{PHL}					7.8	11	1	12.5	
t_{PZH}	OE	Y	C_L = 50 pF		9.1	14.1	1	16	ns
t_{PZL}					9.1	14.1	1	16	
t_{PHZ}	$\overline{OE}$	Y	C_L = 50 pF		10.3	14	1	16	ns
t_{PLZ}					10.3	14	1	16	

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	OUTPUT CAPACITANCE	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
t_{PLH}	A	Y	C_L = 15 pF		3.6	5.5	1	6.5	ns
t_{PHL}					3.6	5.5	1	6.5	
t_{PZH}	$\overline{OE}$	Y	C_L = 15 pF		4.7	7.3	1	8.5	ns
t_{PZL}					4.7	7.3	1	8.5	
t_{PHZ}	$\overline{OE}$	Y	C_L = 15 pF		5.2	7.2	1	8.5	ns
t_{PLZ}					5.2	7.2	1	8.5	
t_{PLH}	A	Y	C_L = 50 pF		5.1	7.5	1	8.5	ns
t_{PHL}					5.1	7.5	1	8.5	
t_{PZH}	$\overline{OE}$	Y	C_L = 50 pF		6.2	9.3	1	10.5	ns
t_{PZL}					6.2	9.3	1	10.5	
t_{PHZ}	$\overline{OE}$	Y	C_L = 50 pF		6.7	9.2	1	10.5	ns
t_{PLZ}					6.7	9.2	1	10.5	

output-skew characteristics, C_L = 50 pF (see Note 4)

PARAMETER		V_{CC}	T_A = 25°C		MIN	MAX	UNIT
			MIN	MAX			
$t_{sk(o)}$	Output skew	3.3 V ± 0.3 V		1.5		1.5	ns
		5 V ± 0.5 V		1		1	

NOTE 4: Characteristics are determined during product characterization and ensured by design.

noise characteristics, V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C (see Note 5)

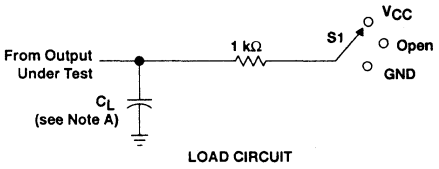
PARAMETER		MIN	TYP	MAX	UNIT
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.6		V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		−0.6		V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}		4.6		V
$V_{IH(D)}$	High-level dynamic input voltage	3.5			V
$V_{IL(D)}$	Low-level dynamic input voltage			1.5	V

NOTE 5: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

operating characteristics, V_{CC} = 5 V, T_A = 25°C

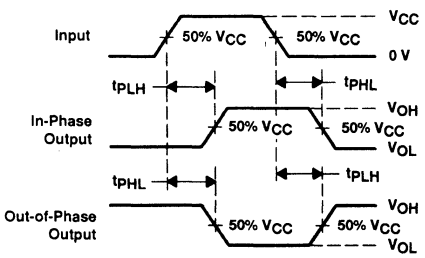
PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	C_L = 50 pF, f = 1 MHz	10	pF

PARAMETER MEASUREMENT INFORMATION

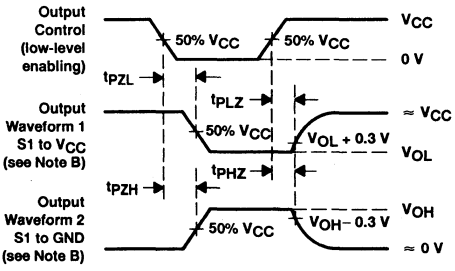


LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND



VOLTAGE WAVEFORMS
DELAY TIMES



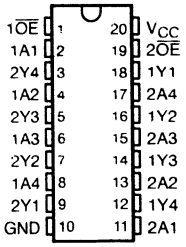
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

- **Operating Range: 2-V to 5.5-V V_{CC}**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **High Latch-Up Immunity Exceeds 300 mA Per JEDEC Standard JESD-17**
- **Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW) Packages, and Standard Plastic (N) DIPs**

DB, DW, N, OR PW PACKAGE
(TOP VIEW)



description

This octal buffer/driver is designed specifically to improve both the performance and density of 3-state memory-address drivers, clock drivers, and bus-oriented receivers and transmitters.

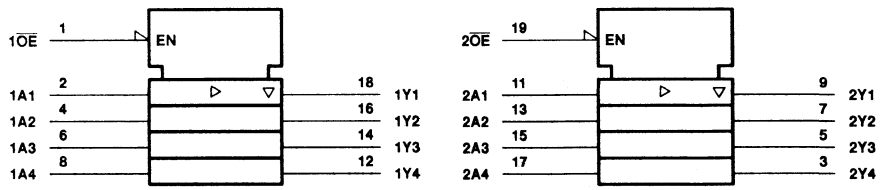
The SN74AHC244 is organized as two 4-bit buffers/line drivers with separate output-enable ($\overline{OE}$) inputs. When $\overline{OE}$ is low, the device passes data from the A inputs to the Y outputs. When $\overline{OE}$ is high, the outputs are in the high-impedance state.

The SN74AHC244 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each buffer)

INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	H
L	L	L
H	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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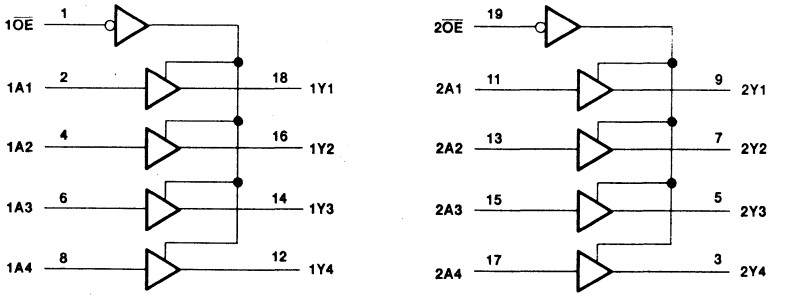
logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... –0.5 V to 7 V
Output voltage range, V_O (see Note 1) ..... –0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) ..... –20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±25 mA
Continuous current through V_{CC} or GND ..... ±75 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2): DB package ..... 0.6 W
DW package ..... 1.6 W
N package ..... 1.3 W
PW package ..... 0.7 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions (see Note 3)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5		V
		V_{CC} = 3 V	2.1		
		V_{CC} = 5.5 V	3.85		
V_{IL}	Low-level input voltage	V_{CC} = 2 V		0.5	V
		V_{CC} = 3 V		0.9	
		V_{CC} = 5.5 V		1.65	
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2 V		–50	μA
		V_{CC} = 3.3 V ± 0.3 V		–4	mA
		V_{CC} = 5 V ± 0.5 V		–8	
I_{OL}	Low-level output current	V_{CC} = 2 V		50	μA
		V_{CC} = 3.3 V ± 0.3 V		4	mA
		V_{CC} = 5 V ± 0.5 V		8	
$\Delta t/\Delta v$	Input transition rise or fall rate	V_{CC} = 3.3 V ± 0.3 V		100	ns/V
		V_{CC} = 5 V ± 0.5 V		20	
T_A	Operating free-air temperature		–40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
V_{OH}		I_{OH} = –50 μA	2 V	1.9	2		1.9		V
			3 V	2.9	3		2.9		
			4.5 V	4.4	4.5		4.4		
		I_{OH} = –4 mA	3 V	2.58			2.48		
		I_{OH} = –8 mA	4.5 V	3.94			3.8		
V_{OL}		I_{OL} = 50 μA	2 V			0.1		0.1	V
			3 V			0.1		0.1	
			4.5 V			0.1		0.1	
		I_{OL} = 4 mA	3 V			0.36		0.44	
		I_{OL} = 8 mA	4.5 V			0.36		0.44	
I_I	Data inputs	V_I = V_{CC} or GND	5.5 V			±0.1		±1	μA
	Control inputs					±0.1		±1	
I_{OZ}		V_O = V_{CC} or GND, V_I ($\overline{OE}$) = V_{IL} or V_{IH}	5.5 V			±0.25		±2.5	μA
I_{CC}		V_I = V_{CC} or GND, I_O = 0	5.5 V			4		40	μA
C_i		V_I = V_{CC} or GND	5 V		2	10		10	pF
C_o		V_O = V_{CC} or GND	5 V		3.5				pF

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	OUTPUT CAPACITANCE	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
t_{PLH}	A	Y	C_L = 15 pF		5.8	8.4	1	10	ns
t_{PHL}					5.8	8.4	1	10	
t_{PZH}	$\overline{OE}$	Y	C_L = 15 pF		6.6	10.6	1	12.5	ns
t_{PZL}					6.6	10.6	1	12.5	
t_{PHZ}	$\overline{OE}$	Y	C_L = 15 pF		5	9.7	1	11	ns
t_{PLZ}					5	9.7	1	11	
t_{PLH}	A	Y	C_L = 50 pF		8.3	11.9	1	13.5	ns
t_{PHL}					8.3	11.9	1	13.5	
t_{PZH}	OE	Y	C_L = 50 pF		9.1	14.1	1	16	ns
t_{PZL}					9.1	14.1	1	16	
t_{PHZ}	OE	Y	C_L = 50 pF		10.3	14	1	16	ns
t_{PLZ}					10.3	14	1	16	

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	OUTPUT CAPACITANCE	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
t_{PLH}	A	Y	C_L = 15 pF		3.9	5.5	1	6.5	ns
t_{PHL}					3.9	5.5	1	6.5	
t_{PZH}	$\overline{OE}$	Y	C_L = 15 pF		4.7	7.3	1	8.5	ns
t_{PZL}					4.7	7.3	1	8.5	
t_{PHZ}	$\overline{OE}$	Y	C_L = 15 pF		5	7.2	1	8.5	ns
t_{PLZ}					5	7.2	1	8.5	
t_{PLH}	A	Y	C_L = 50 pF		5.4	7.5	1	8.5	ns
t_{PHL}					5.4	7.5	1	8.5	
t_{PZH}	$\overline{OE}$	Y	C_L = 50 pF		6.2	9.3	1	10.5	ns
t_{PZL}					6.2	9.3	1	10.5	
t_{PHZ}	$\overline{OE}$	Y	C_L = 50 pF		6.7	9.2	1	10.5	ns
t_{PLZ}					6.7	9.2	1	10.5	

output-skew characteristics, C_L = 50 pF (see Note 4)

PARAMETER		V_{CC}	T_A = 25°C		MIN	MAX	UNIT
			MIN	MAX			
$t_{sk(o)}$	Output skew	3.3 V ± 0.3 V		1.5		1.5	ns
		5 V ± 0.5 V		1		1	

NOTE 4: Characteristics are determined during product characterization and ensured by design.

noise characteristics, V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C (see Note 5)

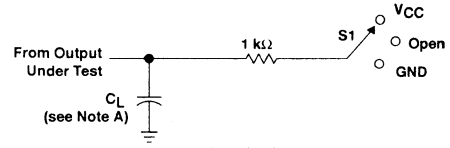
PARAMETER		MIN	TYP	MAX	UNIT
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.5		V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		−0.2		V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}		4.8		V
$V_{IH(D)}$	High-level dynamic input voltage	3.5			V
$V_{IL(D)}$	Low-level dynamic input voltage			1.5	V

NOTE 5: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

operating characteristics, V_{CC} = 5 V, T_A = 25°C

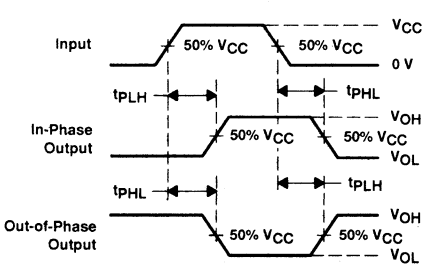
PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	C_L = 50 pF, f = 1 MHz	8.6	pF

PARAMETER MEASUREMENT INFORMATION

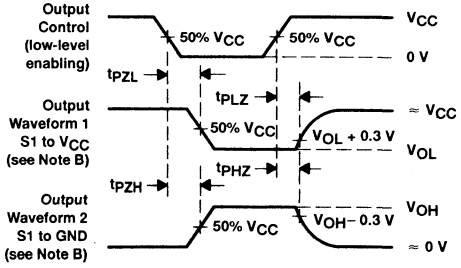


LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND



VOLTAGE WAVEFORMS
DELAY TIMES



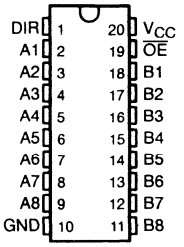
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

- **Operating Range: 2-V to 5.5-V V_{CC}**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **High Latch-Up Immunity Exceeds 300 mA Per JEDEC Standard JESD-17**
- **Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW) Packages, and Standard Plastic (N) DIPs**

DB, DW, N, OR PW PACKAGE
(TOP VIEW)



description

This octal bus transceiver is designed for asynchronous two-way communication between data buses. The control-function implementation minimizes external timing requirements.

The SN74AHC245 allows data transmission from the A bus to the B bus or from the B bus to the A bus, depending upon the logic level at the direction-control (DIR) input. The output-enable ($\overline{OE}$) input can be used to disable the device so that the buses are effectively isolated.

The SN74AHC245 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE

INPUTS		OUTPUT
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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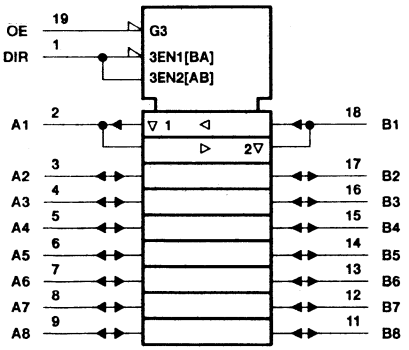
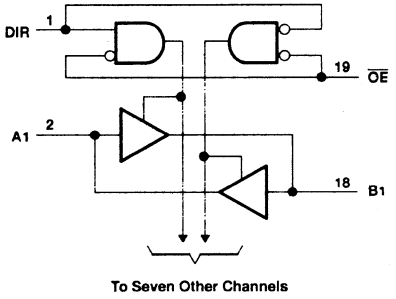
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... –0.5 V to 7 V
Output voltage range, V_O (see Note 1) ..... –0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$) ..... –20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) ..... ±25 mA
Continuous current through V_{CC} or GND ..... ±75 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2): DB package ..... 0.6 W
DW package ..... 1.6 W
N package ..... 1.3 W
PW package ..... 0.7 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions (see Note 3)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5		V
		V_{CC} = 3 V	2.1		
		V_{CC} = 5.5 V	3.85		
V_{IL}	Low-level input voltage	V_{CC} = 2 V		0.5	V
		V_{CC} = 3 V		0.9	
		V_{CC} = 5.5 V		1.65	
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2 V		–50	μA
		V_{CC} = 3.3 V ± 0.3 V		–4	mA
		V_{CC} = 5 V ± 0.5 V		–8	
I_{OL}	Low-level output current	V_{CC} = 2 V		50	μA
		V_{CC} = 3.3 V ± 0.3 V		4	mA
		V_{CC} = 5 V ± 0.5 V		8	
$\Delta t/\Delta v$	Input transition rise or fall rate	V_{CC} = 3.3 V ± 0.3 V		100	ns/V
		V_{CC} = 5 V ± 0.5 V		20	
T_A	Operating free-air temperature		–40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
V_{OH}		I_{OH} = –50 μA	2 V	1.9	2		1.9		V
			3 V	2.9	3		2.9		
			4.5 V	4.4	4.5		4.4		
		I_{OH} = –4 mA	3 V	2.58			2.48		
		I_{OH} = –8 mA	4.5 V	3.94			3.8		
V_{OL}		I_{OL} = 50 μA	2 V			0.1		0.1	V
			3 V			0.1		0.1	
			4.5 V			0.1		0.1	
		I_{OL} = 4 mA	3 V			0.36		0.44	
		I_{OL} = 8 mA	4.5 V			0.36		0.44	
I_I	A or B inputs	V_I = V_{CC} or GND	5.5 V			±0.1		±1	μA
	$\overline{OE}$ or DIR					±0.1		±1	
I_{OZ}†		V_O = V_{CC} or GND, V_I ($\overline{OE}$) = V_{IL} or V_{IH}	5.5 V			±0.25		±2.5	μA
I_{CC}		V_I = V_{CC} or GND, I_O = 0	5.5 V			4		40	μA
C_i	$\overline{OE}$ or DIR inputs	V_I = V_{CC} or GND	5 V		2.5	10		10	pF
C_{io}	A or B inputs	V_I = V_{CC} or GND	5 V		4				pF

† The parameter I_{OZ} includes the input leakage current.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	OUTPUT CAPACITANCE	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
t_{PLH}	A or B	B or A	C_L = 15 pF		5.8	8.4	1	10	ns
t_{PHL}					5.8	8.4	1	10	
t_{PZH}	$\overline{OE}$	A or B	C_L = 15 pF		8.5	13.2	1	15.5	ns
t_{PZL}					8.5	13.2	1	15.5	
t_{PHZ}	$\overline{OE}$	A or B	C_L = 15 pF		8.9	12.5	1	15.5	ns
t_{PLZ}					8.9	12.5	1	15.5	
t_{PLH}	A or B	B or A	C_L = 50 pF		8.3	11.9	1	13.5	ns
t_{PHL}					8.3	11.9	1	13.5	
t_{PZH}	$\overline{OE}$	A or B	C_L = 50 pF		11	16.7	1	19	ns
t_{PZL}					11	16.7	1	19	
t_{PHZ}	OE	A or B	C_L = 50 pF		11.5	15.8	1	18	ns
t_{PLZ}					11.5	15.8	1	18	

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	OUTPUT CAPACITANCE	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
t_{PLH}	A or B	B or A	C_L = 15 pF		4	5.5	1	6.5	ns
t_{PHL}					4	5.5	1	6.5	
t_{PZH}	$\overline{OE}$	A or B	C_L = 15 pF		5.8	8.5	1	10	ns
t_{PZL}					5.8	8.5	1	10	
t_{PHZ}	$\overline{OE}$	A or B	C_L = 15 pF		5.6	7.8	1	9.2	ns
t_{PLZ}					5.6	7.8	1	9.2	
t_{PLH}	A or B	B or A	C_L = 50 pF		5.5	7.5	1	8.5	ns
t_{PHL}					5.5	7.5	1	8.5	
t_{PZH}	$\overline{OE}$	A or B	C_L = 50 pF		7.3	10.6	1	12	ns
t_{PZL}					7.3	10.6	1	12	
t_{PHZ}	$\overline{OE}$	A or B	C_L = 50 pF		7	9.7	1	11	ns
t_{PLZ}					7	9.7	1	11	

output-skew characteristics, C_L = 50 pF (see Note 4)

PARAMETER		V_{CC}	T_A = 25°C		MIN	MAX	UNIT
			MIN	MAX			
$t_{sk(o)}$	Output skew	3.3 V ± 0.3 V		1.5		1.5	ns
		5 V ± 0.5 V		1		1	

NOTE 4: Characteristics are determined during product characterization and ensured by design.

noise characteristics, V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C (see Note 5)

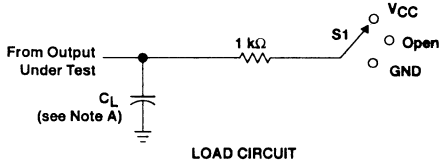
PARAMETER		MIN	TYP	MAX	UNIT
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.9		V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		−0.9		V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}		4.3		V
$V_{IH(D)}$	High-level dynamic input voltage	3.5			V
$V_{IL(D)}$	Low-level dynamic input voltage			1.5	V

NOTE 5: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

operating characteristics, V_{CC} = 5 V, T_A = 25°C

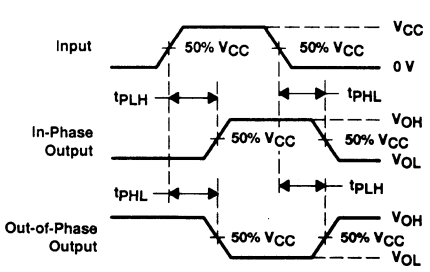
PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per transceiver	C_L = 50 pF, f = 1 MHz	14	pF

PARAMETER MEASUREMENT INFORMATION

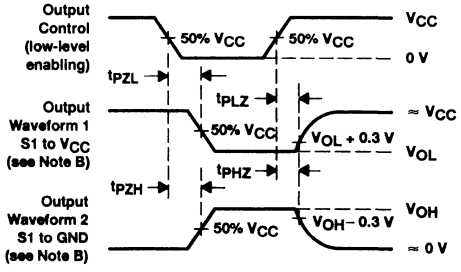


LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND



VOLTAGE WAVEFORMS
DELAY TIMES



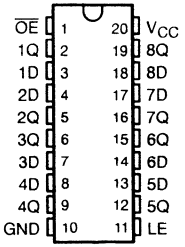
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

- **Operating Range: 2-V to 5.5-V V_{CC}**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW) Packages, and Standard Plastic (N) DIPs**

DB, DW, N, OR PW PACKAGE
(TOP VIEW)



description

The SN74AHC373 is an octal transparent D-type latch.

When the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is low, the Q outputs are latched at the logic levels of the data (D) inputs.

A buffered output-enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.

$\overline{OE}$ does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN74AHC373 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE
(each latch)

INPUTS			OUTPUT
$\overline{OE}$	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

PRODUCT PREVIEW

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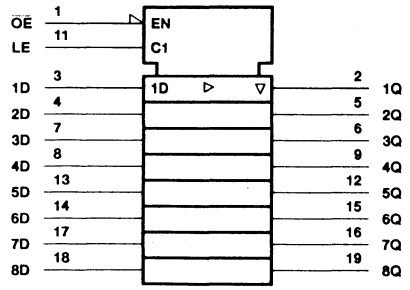
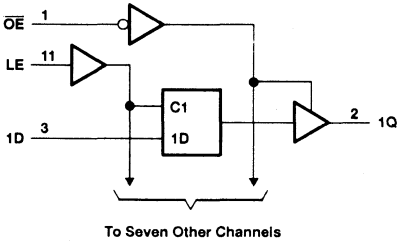
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) ..... − 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ± 20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ± 25 mA
Continuous current through V_{CC} or GND ..... ± 75 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2): DB package ..... 0.6 W
DW package ..... 1.6 W
N package ..... 1.3 W
PW package ..... 0.7 W
Storage temperature range, T_{stg} ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

PRODUCT PREVIEW

recommended operating conditions (see Note 3)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5		V
		V_{CC} = 3 V	2.1		
		V_{CC} = 5.5 V	3.85		
V_{IL}	Low-level input voltage	V_{CC} = 2 V		0.5	V
		V_{CC} = 3 V		0.9	
		V_{CC} = 5.5 V		1.65	
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2 V		– 50	μA
		V_{CC} = 3.3 V ± 0.3 V		– 4	mA
		V_{CC} = 5 V ± 0.5 V		–8	
I_{OL}	Low-level output current	V_{CC} = 2 V		50	μA
		V_{CC} = 3.3 V ± 0.3 V		4	mA
		V_{CC} = 5 V ± 0.5 V		8	
$\Delta t/\Delta v$	Input transition rise or fall rate	V_{CC} = 3.3 V ± 0.3 V		100	ns/V
		V_{CC} = 5 V ± 0.5 V		20	
T_A	Operating free-air temperature		– 40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
V_{OH}	I_{OH} = – 50 μA	2 V	1.9			1.9		V
		3 V	2.9			2.9		
		4.5 V	4.4			4.4		
	I_{OH} = – 4 mA	3 V	2.58			2.48		
	I_{OH} = – 8 mA	4.5 V	3.94			3.8		
V_{OL}	I_{OL} = 50 μA	2 V			0.1		0.1	V
		3 V			0.1		0.1	
		4.5 V			0.1		0.1	
	I_{OL} = 4 mA	3 V			0.36		0.44	
	I_{OL} = 8 mA	4.5 V			0.36		0.44	
I_I	V_I = V_{CC} or GND	5.5 V			± 0.1		± 1	μA
I_{OZ}	V_I = V_{IH} or V_{IL}, V_O = V_{CC} or GND	5.5 V			± 0.25		± 2.5	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			4		40	μA
C_i	V_I = V_{CC} or GND	5 V		4	10		10	pF
C_o		5 V		6				pF

PRODUCT PREVIEW

timing requirements over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

		T_A = 25°C		MIN	MAX	UNIT
		MIN	MAX			
t_w	Pulse duration, $\overline{LE}$ high	5		5		ns
t_{su}	Setup time, data before $\overline{LE}$↓	4		4		ns
t_h	Hold time, data after $\overline{LE}$↓	1		1		ns

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

		T_A = 25°C		MIN	MAX	UNIT
		MIN	MAX			
t_w	Pulse duration, $\overline{LE}$ high	5		5		ns
t_{su}	Setup time, data before $\overline{LE}$↓	4		4		ns
t_h	Hold time, data after $\overline{LE}$↓	1		1		ns

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
t_{PLH}	D	Q	C_L = 15 pF		7.3	11.4	1	13.5	ns
t_{PHL}					7.3	11.4	1	13.5	
t_{PLH}	LE	Q			7	11	1	13	ns
t_{PHL}					7	11	1	13	
t_{PZH}	$\overline{OE}$	Q			7.3	11.4	1	13.5	ns
t_{PZL}					7.3	11.4	1	13.5	
t_{PHZ}	$\overline{OE}$	Q							ns
t_{PLZ}									
t_{PLH}	D	Q	C_L = 50 pF		9.8	14.9	1	17	ns
t_{PHL}					9.8	14.9	1	17	
t_{PLH}	LE	Q			9.5	14.5	1	16.5	ns
t_{PHL}					9.5	14.5	1	16.5	
t_{PZH}	$\overline{OE}$	Q			9.8	14.9	1	17	ns
t_{PZL}					9.8	14.9	1	17	
t_{PHZ}	$\overline{OE}$	Q			9.5	13.2	1	15	ns
t_{PLZ}					9.5	13.2	1	15	

PRODUCT PREVIEW

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
t_{PLH}	D	Q	C_L = 15 pF		5	7.2	1	8.5	ns
t_{PHL}					5	7.2	1	8.5	
t_{PLH}	LE	Q			4.9	7.2	1	8.5	ns
t_{PHL}					4.9	7.2	1	8.5	
t_{PZH}	$\overline{OE}$	Q			5.5	8.1	1	9.5	ns
t_{PZL}					5.5	8.1	1	9.5	
t_{PHZ}	$\overline{OE}$	Q							ns
t_{PLZ}									
t_{PLH}	D	Q	C_L = 50 pF		6.5	9.2	1	10.5	ns
t_{PHL}					6.5	9.2	1	10.5	
t_{PLH}	LE	Q			6.4	9.2	1	10.5	ns
t_{PHL}					6.4	9.2	1	10.5	
t_{PZH}	$\overline{OE}$	Q			7	10.1	1	11.5	ns
t_{PZL}					7	10.1	1	11.5	
t_{PHZ}	$\overline{OE}$	Q			6.5	9.2	1	10.5	ns
t_{PLZ}					6.5	9.2	1	10.5	

output-skew characteristics, C_L = 50 pF (see Note 4)

PARAMETER		V_{CC}	T_A = 25°C		MIN	MAX	UNIT
			MIN	MAX			
$t_{sk(o)}$	Output skew	3.3 V ± 0.3 V		1.5		1.5	ns
		5 V ± 0.5 V		1		1	

NOTE 4: Characteristics are determined during product characterization and ensured by design.

noise characteristics, V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C (see Note 5)

PARAMETER		MIN	TYP	MAX	UNIT
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}			0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}			−0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}				V
$V_{IH(D)}$	High-level dynamic input voltage	3.5			V
$V_{IL(D)}$	Low-level dynamic input voltage			1.5	V

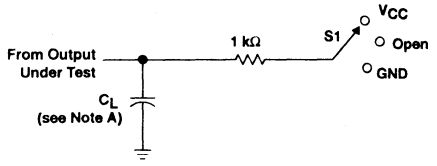
NOTE 5: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
C_{pd}	Power dissipation capacitance	C_L = 50 pF,	f = 1 MHz		27		pF

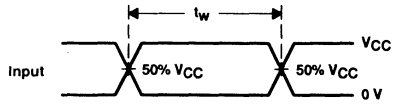
PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

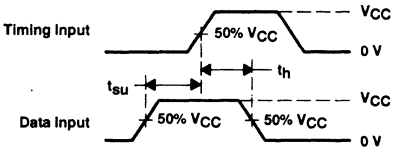


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND

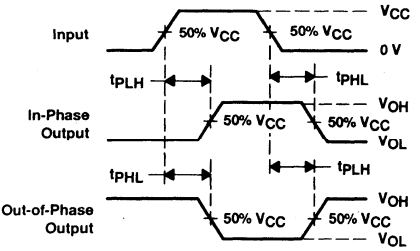
LOAD CIRCUIT



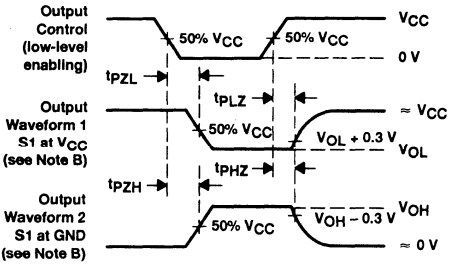
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

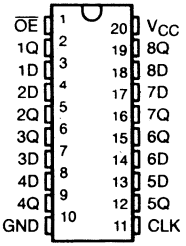
NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PRODUCT PREVIEW

- **Operating Range: 2-V to 5.5-V V_{CC}**
- **3-State Outputs Drive Bus Lines Directly**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW) Packages, and Standard Plastic (N) DIPs**

DB, DW, N, OR PW PACKAGE
(TOP VIEW)



description

The SN74AHC374 is an octal edge-triggered D-type flip-flop that features 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. This device is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

On the positive transition of the clock (CLK) input, the Q outputs are set to the logic levels of the data (D) inputs.

A buffered output-enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without interface or pullup components.

$\overline{OE}$ does not affect internal operations of the flip-flop. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN74AHC374 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each flip-flop)

INPUTS			OUTPUT
$\overline{OE}$	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	H or L	X	Q_0
H	X	X	Z

PRODUCT PREVIEW

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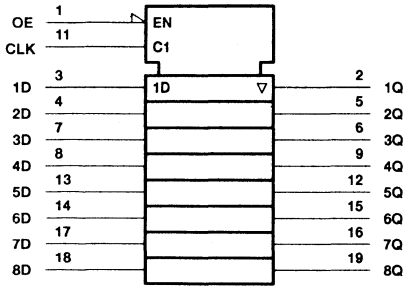
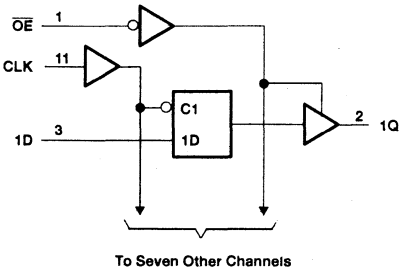
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$) ..... − 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ± 20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ± 25 mA
Continuous current through V_{CC} or GND ..... ± 75 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2): DB package ..... 0.6 W
DW package ..... 1.6 W
N package ..... 1.3 W
PW package ..... 0.7 W
Storage temperature range, T_{stg} ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

PRODUCT PREVIEW

recommended operating conditions (see Note 3)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5		V
		V_{CC} = 3 V	2.1		
		V_{CC} = 5.5 V	3.85		
V_{IL}	Low-level input voltage	V_{CC} = 2 V		0.5	V
		V_{CC} = 3 V		0.9	
		V_{CC} = 5.5 V		1.65	
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2 V		– 50	μA
		V_{CC} = 3.3 V ± 0.3 V		– 4	mA
		V_{CC} = 5 V ± 0.5 V		–8	
I_{OL}	Low-level output current	V_{CC} = 2 V		50	μA
		V_{CC} = 3.3 V ± 0.3 V		4	mA
		V_{CC} = 5 V ± 0.5 V		8	
$\Delta t/\Delta v$	Input transition rise or fall rate	V_{CC} = 3.3 V ± 0.3 V		100	ns/V
		V_{CC} = 5 V ± 0.5 V		20	
T_A	Operating free-air temperature		– 40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
V_{OH}	I_{OH} = – 50 μA	2 V	1.9	2		1.9		V
		3 V	2.9	3		2.9		
		4.5 V	4.4	4.5		4.4		
	I_{OH} = – 4 mA	3 V	2.58			2.48		
	I_{OH} = – 8 mA	4.5 V	3.94			3.8		
V_{OL}	I_{OL} = 50 μA	2 V			0.1		0.1	V
		3 V			0.1		0.1	
		4.5 V			0.1		0.1	
	I_{OL} = 4 mA	3 V			0.36		0.44	
	I_{OL} = 8 mA	4.5 V			0.36		0.44	
I_I	V_I = V_{CC} or GND	5.5 V			± 0.1		± 1	μA
I_{OZ}	V_O = V_{CC} or GND	5.5 V			± 0.25		± 2.5	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			4		40	μA
C_i	V_I = V_{CC} or GND	5 V		4	10		10	pF
C_o	V_O = V_{CC} or GND	5 V		6				pF

PRODUCT PREVIEW

timing requirements over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

		T_A = 25°C		MIN	MAX	UNIT
		MIN	MAX			
t_w	Pulse duration, CLK high or low	5		5.5		ns
t_{su}	Setup time, data before CLK↑	4.5		4		ns
t_h	Hold time, data after CLK↑	2		2		ns

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

		T_A = 25°C		MIN	MAX	UNIT
		MIN	MAX			
t_w	Pulse duration, CLK high or low	5		5		ns
t_{su}	Setup time, data before CLK↑	3		3		ns
t_h	Hold time, data after CLK↑	2		2		ns

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
f_{max}			C_L = 15 pF	80	130		70		MHz
			C_L = 50 pF	55	85		50		
t_{PLH}	CLK	Q	C_L = 15 pF		8.1	12.7	1	15	ns
t_{PHL}					8.1	12.7	1	15	
t_{PZH}	$\overline{OE}$	Q			7.1	11	1	13	ns
t_{PZL}					7.1	11	1	13	
t_{PHZ}	$\overline{OE}$	Q							ns
t_{PLZ}									
t_{PLH}	CLK	Q	C_L = 50 pF		10.6	16.2	1	18.5	ns
t_{PHL}					10.6	16.2	1	18.5	
t_{PZH}	$\overline{OE}$	Q			9.6	14.5	1	16.5	ns
t_{PZL}					9.6	14.5	1	16.5	
t_{PHZ}	$\overline{OE}$	Q			10.2	14	1	16	ns
t_{PLZ}					10.2	14	1	16	

PRODUCT PREVIEW

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
f_{max}			C_L = 15 pF	130	185		110		MHz
			C_L = 50 pF	85	120		75		
t_{PLH}	CLK	Q	C_L = 15 pF		5.4	8.1	1	9.5	ns
t_{PHL}					5.4	8.1	1	9.5	
t_{PZH}	$\overline{OE}$	Q			5.1	7.6	1	9	ns
t_{PZL}					5.1	7.6	1	9	
t_{PHZ}	$\overline{OE}$	Q							ns
t_{PLZ}									
t_{PLH}	CLK	Q	C_L = 50 pF		6.9	10.1	1	11.5	ns
t_{PHL}					6.9	10.1	1	11.5	
t_{PZH}	$\overline{OE}$	Q			6.6	9.6	1	11	ns
t_{PZL}					6.6	9.6	1	11	
t_{PHZ}	$\overline{OE}$	Q			6.1	8.8	1	10	ns
t_{PLZ}					6.1	8.8	1	10	

output-skew characteristics, C_L = 50 pF (see Note 4)

PARAMETER		V_{CC}	T_A = 25°C		MIN	MAX	UNIT
			MIN	MAX			
$t_{sk(o)}$	Output skew	3.3 V ± 0.3 V		1.5		1.5	ns
		5 V ± 0.5 V		1		1	

NOTE 4: Characteristics are determined during product characterization and ensured by design.

noise characteristics, V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C (see Note 5)

PARAMETER		MIN	TYP	MAX	UNIT
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}			0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}			−0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}				V
$V_{IH(D)}$	High-level dynamic input voltage	3.5			V
$V_{IL(D)}$	Low-level dynamic input voltage			1.5	V

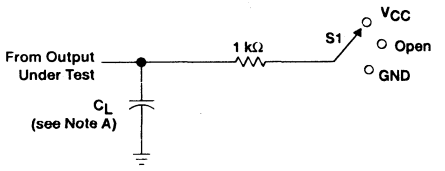
NOTE 5: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_{pd}	Power dissipation capacitance	C_L = 50 pF, f = 1 MHz		32		pF

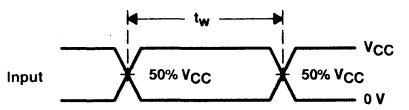
PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

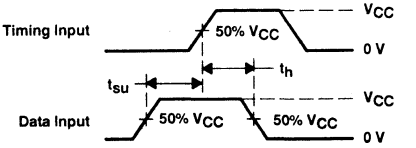


LOAD CIRCUIT

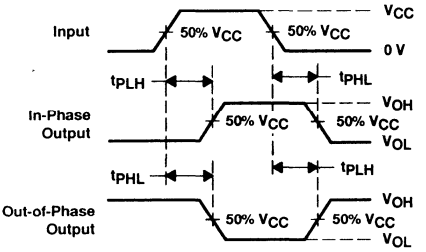
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND



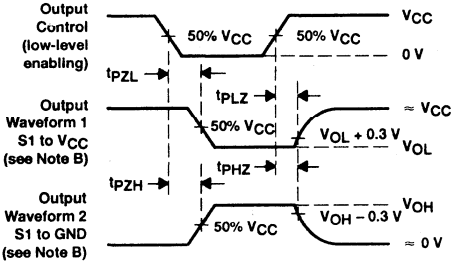
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

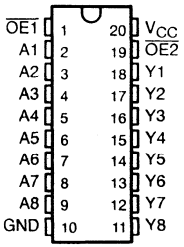
NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PRODUCT PREVIEW

- **Operating Range: 2-V to 5.5-V V_{CC}**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW) Packages, and Standard Plastic (N) DIPs**

DB, DW, N, OR PW PACKAGE
(TOP VIEW)



description

The SN74AHC540 octal buffer/driver is ideal for driving bus lines or buffer memory address registers. This device features inputs and outputs on opposite sides of the package to facilitate printed-circuit-board layout.

The 3-state control gate is a 2-input AND gate with active-low inputs so that if either output-enable ($\overline{OE1}$ or $\overline{OE2}$) input is high, all corresponding outputs are in the high-impedance state. The outputs provide inverted data when they are not in the high-impedance state.

The SN74AHC540 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE

INPUTS			OUTPUT
$\overline{OE1}$	$\overline{OE2}$	A	Y
L	L	L	H
L	L	H	L
H	X	X	Z
X	H	X	Z

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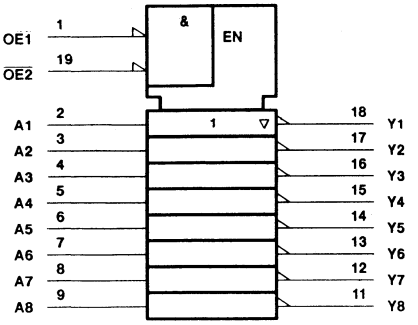
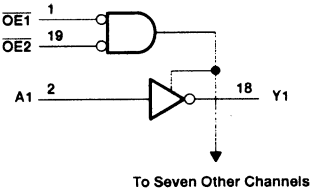
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) ..... − 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ± 20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ± 25 mA
Continuous current through V_{CC} or GND ..... ± 75 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2): DB package ..... 0.6 W
DW package ..... 1.6 W
N package ..... 1.3 W
PW package ..... 0.7 W
Storage temperature range, T_{stg} ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

PRODUCT PREVIEW

recommended operating conditions (see Note 3)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5		V
		V_{CC} = 3 V	2.1		
		V_{CC} = 5.5 V	3.85		
V_{IL}	Low-level input voltage	V_{CC} = 2 V		0.5	V
		V_{CC} = 3 V		0.9	
		V_{CC} = 5.5 V		1.65	
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2 V		– 50	μA
		V_{CC} = 3.3 V ± 0.3 V		– 4	mA
		V_{CC} = 5 V ± 0.5 V		–8	
I_{OL}	Low-level output current	V_{CC} = 2 V		50	μA
		V_{CC} = 3.3 V ± 0.3 V		4	mA
		V_{CC} = 5 V ± 0.5 V		8	
$\Delta t/\Delta v$	Input transition rise or fall rate	V_{CC} = 3.3 V ± 0.3 V		100	ns/V
		V_{CC} = 5 V ± 0.5 V		20	
T_A	Operating free-air temperature		– 40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
V_{OH}		I_{OH} = – 50 μA	2 V	1.9	2		1.9		V
			3 V	2.9	3		2.9		
			4.5 V	4.4	4.5		4.4		
		I_{OH} = – 4 mA	3 V	2.58			2.48		
		I_{OH} = – 8 mA	4.5 V	3.94			3.8		
V_{OL}		I_{OL} = 50 μA	2 V			0.1		0.1	V
			3 V			0.1		0.1	
			4.5 V			0.1		0.1	
		I_{OL} = 4 mA	3 V			0.36		0.44	
		I_{OL} = 8 mA	4.5 V			0.36		0.44	
I_I	Data inputs	V_I = V_{CC} or GND	5.5 V			± 0.1		± 1	μA
	Control inputs					± 0.1		± 1	
I_{OZ}†		V_O = V_{CC} or GND, V_I ($\overline{OE}$) = V_{IL} or V_{IH}	5.5 V			± 0.25		± 2.5	μA
I_{CC}		V_I = V_{CC} or GND, I_O = 0	5.5 V			4		40	μA
C_i		V_I = V_{CC} or GND	5 V		4	10		10	pF
C_o		V_I = V_{CC} or GND	5 V		6				pF

† For I/O pins, the parameter I_{OZ} includes the input leakage current.

PRODUCT PREVIEW

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
t_{PLH}	A	Y	C_L = 15 pF		4.8	7	1	8.5	ns
t_{PHL}					4.8	7	1	8.5	
t_{PZH}	$\overline{OE}$	Y			6.8	10.5	1	12.5	ns
t_{PZL}					6.8	10.5	1	12.5	
t_{PHZ}	$\overline{OE}$	Y							ns
t_{PLZ}									
t_{PLH}	A	Y	C_L = 50 pF		7.3	10.5	1	12	ns
t_{PHL}					7.3	10.5	1	12	
t_{PZH}	$\overline{OE}$	Y			9.3	14	1	16	ns
t_{PZL}					9.3	14	1	16	
t_{PHZ}	$\overline{OE}$	Y			11.2	15.4	1	17.5	ns
t_{PLZ}					11.2	15.4	1	17.5	

PRODUCT PREVIEW

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
t_{PLH}	A	Y	C_L = 15 pF		3.7	5	1	6	ns
t_{PHL}					3.7	5	1	6	
t_{PZH}	$\overline{OE}$	Y			4.7	7.2	1	8.5	ns
t_{PZL}					4.7	7.2	1	8.5	
t_{PHZ}	$\overline{OE}$	Y							ns
t_{PLZ}									
t_{PLH}	A	Y	C_L = 50 pF		5.2	7	1	8	ns
t_{PHL}					5.2	7	1	8	
t_{PZH}	$\overline{OE}$	Y			6.2	9.2	1	10.5	ns
t_{PZL}					6.2	9.2	1	10.5	
t_{PHZ}	$\overline{OE}$	Y			6	8.8	1	10	ns
t_{PLZ}					6	8.8	1	10	

output-skew characteristics, C_L = 50 pF (see Note 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
$t_{sk(o)}$	A	Y	3.3 V ± 0.3 V			1.5		1.5	ns
			5 V ± 0.5 V			1		1	

NOTE 4: Characteristics are determined during product characterization and ensured by design.

noise characteristics, V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C (see Note 5)

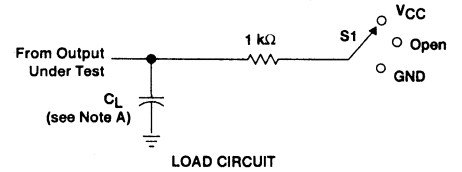
PARAMETER		MIN	TYP	MAX	UNIT
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}			0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}			−0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}				V
$V_{IH(D)}$	High-level dynamic input voltage	3.5			V
$V_{IL(D)}$	Low-level dynamic input voltage			1.5	V

NOTE 5: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

operating characteristics, V_{CC} = 5 V, T_A = 25°C

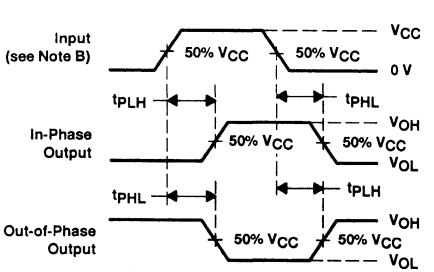
PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
C_{pd}	Power dissipation capacitance	C_L = 50 pF,	f = 1 MHz				pF

PARAMETER MEASUREMENT INFORMATION

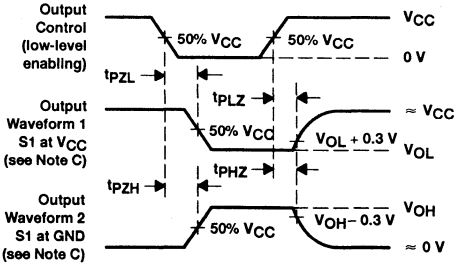


LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND



VOLTAGE WAVEFORMS
DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

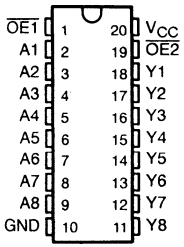
NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PRODUCT PREVIEW

- **Operating Range: 2-V to 5.5-V V_{CC}**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW) Packages, and Standard Plastic (N) DIPs**

DB, DW, N, OR PW PACKAGE
(TOP VIEW)



description

The SN74AHC541 octal buffer/driver is ideal for driving bus lines or buffer memory address registers. This device features inputs and outputs on opposite sides of the package to facilitate printed-circuit-board layout.

The 3-state control gate is a 2-input AND gate with active-low inputs so that if either output-enable ($\overline{OE1}$ or $\overline{OE2}$) input is high, all corresponding outputs are in the high-impedance state. The outputs provide noninverted data when they are not in the high-impedance state.

The SN74AHC541 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE

INPUTS			OUTPUT
$\overline{OE1}$	$\overline{OE2}$	A	Y
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

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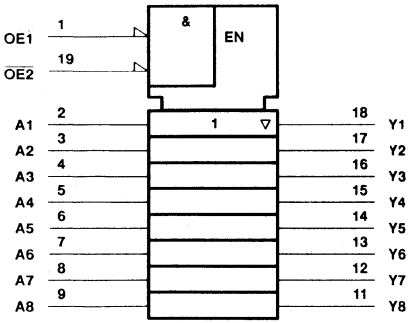
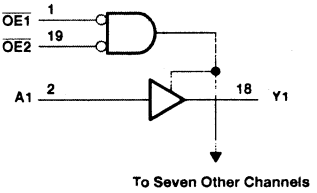
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC}	−0.5 V to 7 V
Input voltage range, V_I (see Note 1)	−0.5 V to 7 V
Output voltage range, V_O (see Note 1)	−0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	± 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	± 20 mA
Continuous output current, I_O (V_O = 0 to V_{CC})	± 25 mA
Continuous current through V_{CC} or GND	± 75 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2): DB package	0.6 W
DW package	1.6 W
N package	1.3 W
PW package	0.7 W
Storage temperature range, T_{stg}	−65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

PRODUCT PREVIEW

recommended operating conditions (see Note 3)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5		V
		V_{CC} = 3 V	2.1		
		V_{CC} = 5.5 V	3.85		
V_{IL}	Low-level input voltage	V_{CC} = 2 V		0.5	V
		V_{CC} = 3 V		0.9	
		V_{CC} = 5.5 V		1.65	
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2 V		– 50	μA
		V_{CC} = 3.3 ± 0.3 V		– 4	mA
		V_{CC} = 5 ± 0.5 V		–8	
I_{OL}	Low-level output current	V_{CC} = 2 V		50	μA
		V_{CC} = 3.3 ± 0.3 V		4	mA
		V_{CC} = 5 ± 0.5 V		8	
$\Delta t/\Delta v$	Input transition rise or fall rate	V_{CC} = 3.3 ± 0.3 V		100	ns/V
		V_{CC} = 5 ± 0.5 V		20	
T_A	Operating free-air temperature		– 40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
V_{OH}		I_{OH} = – 50 μA	2 V	1.9	2		1.9		V
			3 V	2.9	3		2.9		
			4.5 V	4.4	4.5		4.4		
		I_{OH} = – 4 mA	3 V	2.58			2.48		
		I_{OH} = – 8 mA	4.5 V	3.94			3.8		
V_{OL}		I_{OL} = 50 μA	2 V			0.1		0.1	V
			3 V			0.1		0.1	
			4.5 V			0.1		0.1	
		I_{OL} = 4 mA	3 V			0.36		0.44	
		I_{OL} = 8 mA	4.5 V			0.36		0.44	
I_I	Data inputs	V_I = V_{CC} or GND	5.5 V			± 0.1		± 1	μA
	Control inputs					± 0.1		± 1	
I_{OZ}†		V_O = V_{CC} or GND, V_I ($\overline{OE}$) = V_{IL} or V_{IH}	5.5 V			± 0.25		± 2.5	μA
I_{CC}		V_I = V_{CC} or GND, I_O = 0	5.5 V			4		40	μA
C_i		V_I = V_{CC} or GND	5 V		4	10		10	pF
C_o		V_I = V_{CC} or GND	5 V		6				pF

† For input and ouput, I_{OZ} includes the input leakage current.

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switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
t_{PLH}	A	Y	C_L = 15 pF		5	7	1	8.5	ns
t_{PHL}					5	7	1	8.5	
t_{PZH}	OE	Y			6.8	10.5	1	12.5	ns
t_{PZL}					6.8	10.5	1	12.5	
t_{PHZ}	OE	Y							ns
t_{PLZ}									
t_{PLH}	A	Y	C_L = 50 pF		7.5	10.5	1	12	ns
t_{PHL}					7.5	10.5	1	12	
t_{PZH}	$\overline{OE}$	Y			9.3	14	1	16	ns
t_{PZL}					9.3	14	1	16	
t_{PHZ}	$\overline{OE}$	Y			11.2	15.4	1	17.5	ns
t_{PLZ}					11.2	15.4	1	17.5	

PRODUCT PREVIEW

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
t_{PLH}	A	Y	C_L = 15 pF		3.5	5	1	6	ns
t_{PHL}					3.5	5	1	6	
t_{PZH}	$\overline{OE}$	Y			4.7	7.2	1	8.5	ns
t_{PZL}					4.7	7.2	1	8.5	
t_{PHZ}	$\overline{OE}$	Y							ns
t_{PLZ}									
t_{PLH}	A	Y	C_L = 50 pF		5	7	1	8	ns
t_{PHL}					5	7	1	8	
t_{PZH}	$\overline{OE}$	Y			6.2	9.2	1	10.5	ns
t_{PZL}					6.2	9.2	1	10.5	
t_{PHZ}	$\overline{OE}$	Y			6	8.8	1	10	ns
t_{PLZ}					6	8.8	1	10	

output-skew characteristics, C_L = 50 pF (see Note 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
$t_{sk(o)}$	A	Y	3.3 V ± 0.3 V			1.5		1.5	ns
			5 V ± 0.5 V			1		1	

NOTE 4: Characteristics are determined during product characterization and ensured by design.

noise characteristics, V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C (see Note 5)

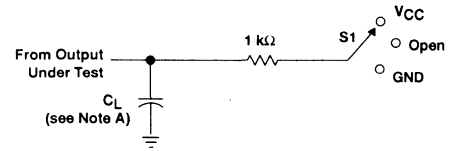
PARAMETER		MIN	TYP	MAX	UNIT
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}			0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}			−0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}				V
$V_{IH(D)}$	High-level dynamic input voltage	3.5			V
$V_{IL(D}$	Low-level dynamic input voltage			1.5	V

NOTE 5. Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

operating characteristics, V_{CC} = 5 V, T_A = 25°C

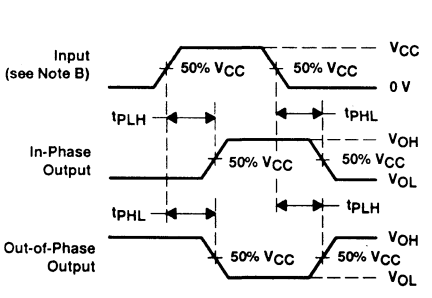
PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	C_L = 50 pF, f = 1 MHz		pF

PARAMETER MEASUREMENT INFORMATION

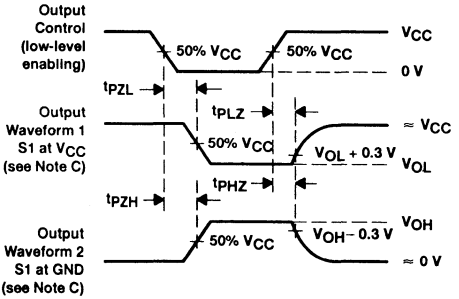


LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND



VOLTAGE WAVEFORMS
DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

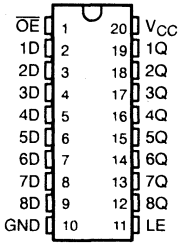
NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PRODUCT PREVIEW

- **3-State Outputs Directly Drive Bus Lines**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW) Packages, and Standard Plastic (N) DIPs**

DB, DW, N, OR PW PACKAGE
(TOP VIEW)



description

The SN74AHC573 is an octal transparent D-type latch.

When the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is low, the Q outputs are latched at the logic levels of the D inputs.

A buffered output-enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.

$\overline{OE}$ does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN74AHC573 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each latch)

INPUTS			OUTPUT
$\overline{OE}$	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

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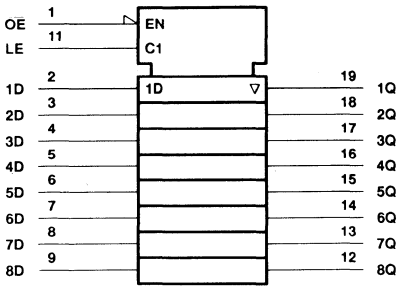
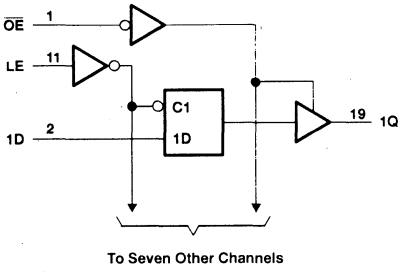
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$) ..... − 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ± 20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) ..... ± 25 mA
Continuous current through V_{CC} or GND ..... ± 75 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2): DB package ..... 0.6 W
DW package ..... 1.6 W
N package ..... 1.3 W
PW package ..... 0.7 W
Storage temperature range, T_{stg} ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

PRODUCT PREVIEW

recommended operating conditions (see Note 3)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5		V
		V_{CC} = 3 V	2.1		
		V_{CC} = 5.5 V	3.85		
V_{IL}	Low-level input voltage	V_{CC} = 2 V		0.5	V
		V_{CC} = 3 V		0.9	
		V_{CC} = 5.5 V		1.65	
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2 V		– 50	μA
		V_{CC} = 3.3 V ± 0.3 V		– 4	mA
		V_{CC} = 5 V ± 0.5 V		–8	
I_{OL}	Low-level output current	V_{CC} = 2 V		50	μA
		V_{CC} = 3.3 V ± 0.3 V		4	mA
		V_{CC} = 5 V ± 0.5 V		8	
$\Delta t/\Delta v$	Input transition rise or fall rate	V_{CC} = 3.3 V ± 0.3 V		100	ns/V
		V_{CC} = 5 V ± 0.5 V		20	
T_A	Operating free-air temperature		– 40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
V_{OH}	I_{OH} = – 50 μA		2 V	1.9	2		1.9		V
			3 V	2.9	3		2.9		
			4.5 V	4.4	4.5		4.4		
	I_{OH} = – 4 mA		3 V	2.58			2.48		
	I_{OH} = – 8 mA		4.5 V	3.94			3.8		
V_{OL}	I_{OL} = 50 μA		2 V			0.1		0.1	V
			3 V			0.1		0.1	
			4.5 V			0.1		0.1	
	I_{OL} = 4 mA		3 V			0.36		0.44	
	I_{OL} = 8 mA		4.5 V			0.36		0.44	
I_I	V_I = V_{CC} or GND		5.5 V			± 0.1		± 1	μA
I_{OZ}	V_I = V_{IL} or V_{IH},	V_O = V_{CC} or GND	5.5 V			± 0.25		2.5	μA
I_{CC}	V_I = V_{CC} or GND,	I_O = 0	5.5 V			4		40	μA
C_i	V_I = V_{CC} or GND		5 V		4	10		10	pF
C_o	V_I = V_{CC} or GND		5 V		6				

PRODUCT PREVIEW

timing requirements over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

		T_A = 25°C		MIN	MAX	UNIT
		MIN	MAX			
t_w	Pulse duration, $\overline{LE}$ high	5		5		ns
t_{su}	Setup time, data before $\overline{LE}\downarrow$	3.5		3.5		ns
t_h	Hold time, data after $\overline{LE}\downarrow$	1.5		1.5		ns

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

		T_A = 25°C		MIN	MAX	UNIT
		MIN	MAX			
t_w	Pulse duration, $\overline{LE}$ high	5		5		ns
t_{su}	Setup time, data before $\overline{LE}\downarrow$	3.5		3.5		ns
t_h	Hold time, data after $\overline{LE}\downarrow$	1.5		1.5		ns

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
t_{PLH}	D	Q	C_L = 15 pF		7	11	1	13	ns
t_{PHL}					7	11	1	13	
t_{PLH}	LE	Q			7.6	11.9	1	14	ns
t_{PHL}					7.6	11.9	1	14	
t_{PZH}	$\overline{OE}$	Q			7.3	11.5	1	13.5	ns
t_{PZL}					7.3	11.5	1	13.5	
t_{PHZ}	$\overline{OE}$	Q							ns
t_{PLZ}									
t_{PLH}	D	Q	C_L = 50 pF		9.5	14.5	1	16.5	ns
t_{PHL}					9.5	14.5	1	16.5	
t_{PLH}	LE	Q			10.1	15.4	1	17.5	ns
t_{PHL}					10.1	15.4	1	17.5	
t_{PZH}	$\overline{OE}$	Q			9.8	15	1	17	ns
t_{PZL}					9.8	15	1	17	
t_{PHZ}	$\overline{OE}$	Q			10.7	14.5	1	16.5	ns
t_{PLZ}					10.7	14.5	1	16.5	

PRODUCT PREVIEW

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
t_{PLH}	D	Q	C_L = 15 pF		4.5	6.8	1	8	ns
t_{PHL}					4.5	6.8	1	8	
t_{PLH}	LE	Q			5	7.7	1	9	ns
t_{PHL}					5	7.7	1	9	
t_{PZH}	$\overline{OE}$	Q			5.2	7.7	1	9	ns
t_{PZL}					5.2	7.7	1	9	
t_{PHZ}	$\overline{OE}$	Q							ns
t_{PLZ}									
t_{PLH}	D	Q	C_L = 50 pF		6	8.8	1	10	ns
t_{PHL}					6	8.8	1	10	
t_{PLH}	LE	Q			6.5	9.7	1	11	ns
t_{PHL}					6.5	9.7	1	11	
t_{PZH}	$\overline{OE}$	Q			6.7	9.7	1	11	ns
t_{PZL}					6.7	9.7	1	11	
t_{PHZ}	$\overline{OE}$	Q			6.7	9.7	1	11	ns
t_{PLZ}					6.7	9.7	1	11	

output-skew characteristics, C_L = 50 pF (see Note 4)

PARAMETER		V_{CC}	T_A = 25°C		MIN	MAX	UNIT
			MIN	MAX			
$t_{sk(o)}$	Output skew	3.3 V ± 0.3 V		1.5		1.5	ns
		5 V ± 0.5 V		1		1	

NOTE 4: Characteristics are determined during product characterization and ensured by design.

noise characteristics, V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C (see Note 5)

PARAMETER		MIN	TYP	MAX	UNIT
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}			0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}			−0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}				V
$V_{IH(D)}$	High-level dynamic input voltage	3.5			V
$V_{IL(D)}$	Low-level dynamic input voltage			1.5	V

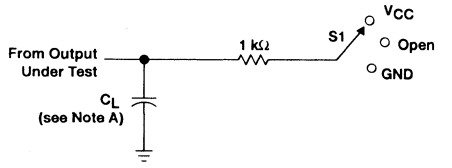
NOTE 5: Characteristics are determined during product characterization and ensured by design and for surface-mount packages only.

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	C_L = 50 pF, f = 1 MHz	29	pF

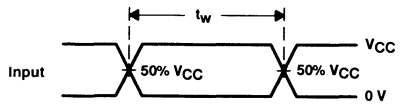
PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

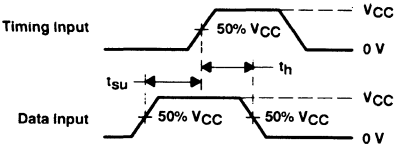


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND

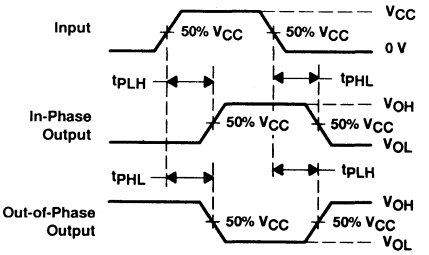
LOAD CIRCUIT



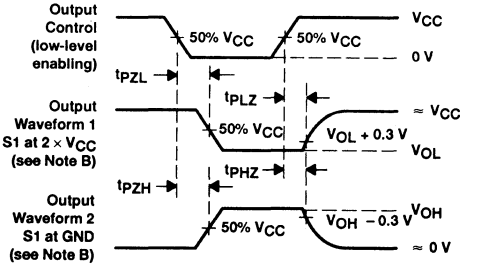
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PRODUCT PREVIEW

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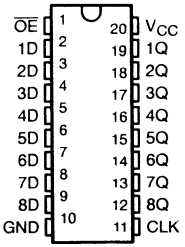
- **Operating Range: 2-V to 5.5-V V_{CC}**
- **3-State Outputs Directly Drive Bus Lines**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW) Packages, and Standard Plastic (N) DIPs**

DB, DW, N, OR PW PACKAGE
(TOP VIEW)



description

The SN74AHC574 is an octal edge-triggered D-type flip-flop that features 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. This device is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

On the positive transition of the clock (CLK) input, the Q outputs are set to the logic levels of the data (D) inputs.

A buffered output-enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without interface or pullup components.

$\overline{OE}$ does not affect internal operations of the flip-flop. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN74AHC574 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each flip-flop)

INPUTS			OUTPUT
$\overline{OE}$	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	H or L	X	Q_0
H	X	X	Z

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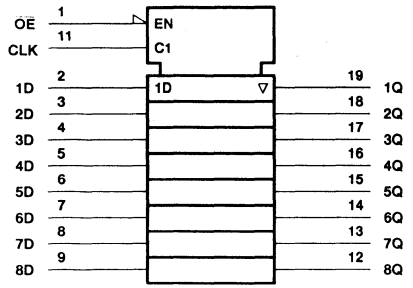
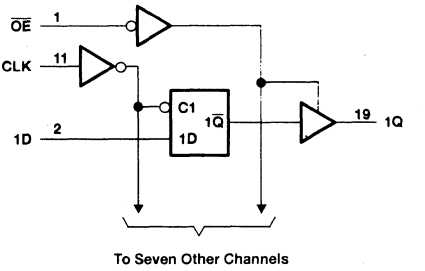
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$) ..... − 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ± 20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ± 25 mA
Continuous current through V_{CC} or GND ..... ± 75 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2): DB package ..... 0.6 W
DW package ..... 1.6 W
N package ..... 1.3 W
PW package ..... 0.7 W
Storage temperature range, T_{stg} ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

PRODUCT PREVIEW

recommended operating conditions (see Note 3)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5		V
		V_{CC} = 3 V	2.1		
		V_{CC} = 5.5 V	3.85		
V_{IL}	Low-level input voltage	V_{CC} = 2 V		0.5	V
		V_{CC} = 3 V		0.9	
		V_{CC} = 5.5 V		1.65	
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2 V		– 50	μA
		V_{CC} = 3.3 V ± 0.3 V		– 4	mA
		V_{CC} = 5 V ± 0.5 V		–8	
I_{OL}	Low-level output current	V_{CC} = 2 V		50	μA
		V_{CC} = 3.3 V ± 0.3 V		4	mA
		V_{CC} = 5 V ± 0.5 V		8	
$\Delta t/\Delta v$	Input transition rise or fall rate	V_{CC} = 3.3 V ± 0.3 V		100	ns/V
		V_{CC} = 5 V ± 0.5 V		20	
T_A	Operating free-air temperature		– 40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
V_{OH}	I_{OH} = – 50 μA	2 V	1.9	2		1.9		V
		3 V	2.9	3		2.9		
		4.5 V	4.4	4.5		4.4		
	I_{OH} = – 4 mA	3 V	2.58			2.48		
	I_{OH} = – 8 mA	4.5 V	3.94			3.8		
V_{OL}	I_{OL} = 50 μA	2 V			0.1		0.1	V
		3 V			0.1		0.1	
		4.5 V			0.1		0.1	
	I_{OL} = 4 mA	3 V			0.36		0.44	
	I_{OL} = 8 mA	4.5 V			0.36		0.44	
I_I	V_I = V_{CC} or GND	5.5 V			± 0.1		± 1	μA
I_{OZ}	V_O = V_{CC} or GND	5.5 V			± 0.25		± 2.5	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			4		40	μA
C_i	V_I = V_{CC} or GND	5 V		4	10		10	pF
C_o	V_O = V_{CC} or GND	5 V		6				pF

PRODUCT PREVIEW

timing requirements over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

		T_A = 25°C		MIN	MAX	UNIT
		MIN	MAX			
t_w	Pulse duration, CLK high or low	5		5.5		ns
t_{su}	Setup time, data before CLK↑	3.5		3.5		ns
t_h	Hold time, data after CLK↑	1.5		1.5		ns

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

		T_A = 25°C		MIN	MAX	UNIT
		MIN	MAX			
t_w	Pulse duration, CLK high or low	5		5		ns
t_{su}	Setup time, data before CLK↑	3.5		3.5		ns
t_h	Hold time, data after CLK↑	1.5		1.5		ns

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
f_{max}			C_L = 15 pF	80	125		65		MHz
			C_L = 50 pF	50	75		45		
t_{PLH}	CLK	Q	C_L = 15 pF		8.5	13.2	1	15.5	ns
t_{PHL}					8.5	13.2	1	15.5	
t_{PZH}	$\overline{OE}$	Q			8.2	12.8	1	15	ns
t_{PZL}					8.2	12.8	1	15	
t_{PHZ}	$\overline{OE}$	Q							ns
t_{PLZ}									
t_{PLH}	CLK	Q	C_L = 50 pF		11	16.7	1	19	ns
t_{PHL}					11	16.7	1	19	
t_{PZH}	$\overline{OE}$	Q			10.7	16.3	1	18.5	ns
t_{PZL}					10.7	16.3	1	18.5	
t_{PHZ}	$\overline{OE}$	Q			11	15	1	17	ns
t_{PLZ}					11	15	1	17	

PRODUCT PREVIEW

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
f_{max}			C_L = 15 pF	130	180		110		MHz
			C_L = 50 pF	85	115		75		
t_{PLH}	CLK	Q	C_L = 15 pF		5.6	8.6	1	10	ns
t_{PHL}					5.6	8.6	1	10	
t_{PZH}	$\overline{OE}$	Q			5.9	9	1	10.5	ns
t_{PZL}					5.9	9	1	10.5	
t_{PHZ}	$\overline{OE}$	Q							ns
t_{PLZ}									
t_{PLH}	CLK	Q	C_L = 50 pF		7.1	10.6	1	12	ns
t_{PHL}					7.1	10.6	1	12	
t_{PZH}	$\overline{OE}$	Q			7.4	11	1	12.5	ns
t_{PZL}					7.4	11	1	12.5	
t_{PHZ}	$\overline{OE}$	Q			7.1	10.1	1	11.5	ns
t_{PLZ}					7.1	10.1	1	11.5	

output-skew characteristics, C_L = 50 pF (see Note 4)

PARAMETER		V_{CC}	T_A = 25°C		MIN	MAX	UNIT
			MIN	MAX			
$t_{sk(o)}$	Output skew	3.3 V ± 0.3 V		1.5		1.5	ns
		5 V ± 0.5 V		1		1	

NOTE 4: Characteristics are determined during product characterization and ensured by design.

noise characteristics, V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C (see Note 5)

PARAMETER		MIN	TYP	MAX	UNIT
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}			0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}			−0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}				V
$V_{IH(D)}$	High-level dynamic input voltage	3.5			V
$V_{IL(D)}$	Low-level dynamic input voltage			1.5	V

NOTE 5: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_{pd}	Power dissipation capacitance	C_L = 50 pF, f = 1 MHz		28		pF

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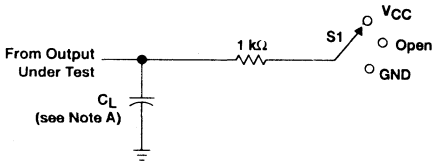
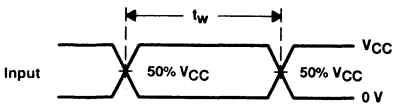
PARAMETER MEASUREMENT INFORMATION

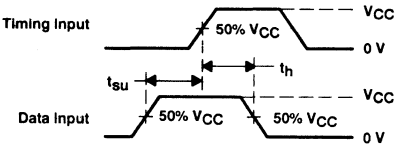


LOAD CIRCUIT

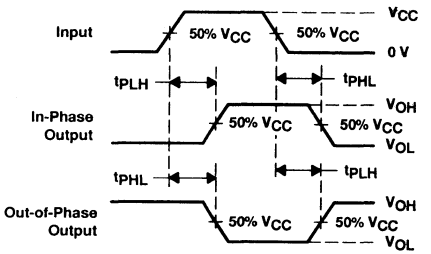
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND



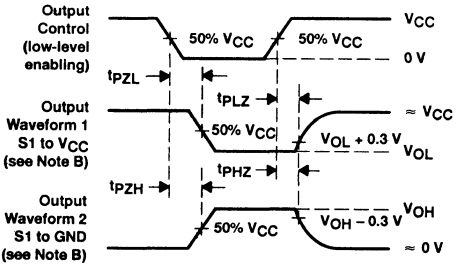
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PRODUCT PREVIEW

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AHCT04 Qualification Data B
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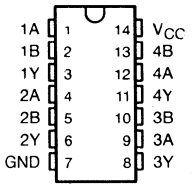
- Inputs Are TTL-Voltage Compatible
- *EPIC*™ (Enhanced-Performance Implanted CMOS) Process
- High Latch-Up Immunity Exceeds 300 mA Per JEDEC Standard JESD-17
- Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW) Packages, and Standard Plastic (N) DIP

D, DB, N, OR PW PACKAGE
(TOP VIEW)



description

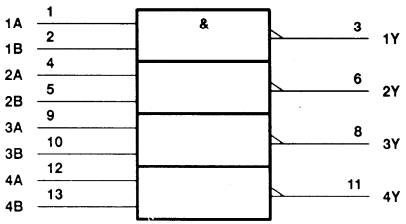
The SN74AHCT00 performs the Boolean functions $Y = \overline{A \bullet B}$ or $Y = \overline{A} + \overline{B}$ in positive logic.

The SN74AHCT00 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE
(each gate)

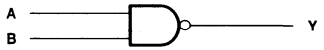
INPUTS		OUTPUT
A	B	Y
H	H	L
L	X	H
X	L	H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) ..... − 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... − 20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ± 25 mA
Continuous current through V_{CC} or GND ..... ± 50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2): D package ..... 1.25 W
DB or PW package ..... 0.5 W
N package ..... 1.1 W
Storage temperature range, T_{stg} ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES. 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4.5	5.5	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
V_I	Input voltage	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	V
I_{OH}	High-level output current		−8	mA
I_{OL}	Low-level output current		8	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		20	ns/V
T_A	Operating free-air temperature	−40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
V_{OH}	I_{OH} = − 50 μA		4.5 V	3.15	3.65		3.15		V
	I_{OH} = − 8 mA			2.5			2.4		
V_{OL}	I_{OL} = 50 μA		4.5 V			0.1		0.1	V
	I_{OL} = 8 mA					0.36		0.44	
I_I	$V_I = V_{CC}$ or GND		5.5 V			± 0.1		± 1	μA
I_{CC}	$V_I = V_{CC}$ or GND,	I_O = 0	5.5 V			2		20	μA
ΔI_{CC}‡	One input at 3.4 V,	Other inputs at V_{CC} or GND	5.5 V			1.35		1.5	mA
I_{off}	V_O = 5.5 V		0 V			0.5		5	μA
C_i	$V_I = V_{CC}$ or GND		5 V		2	10		10	pF

‡ This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C		MIN	MAX	UNIT
				MIN	TYP MAX			
t_{PLH}	A or B	Y	C_L = 15 pF		5 6.9	1	8	ns
t_{PHL}					5 6.9	1	8	
t_{PLH}	A or B	Y	C_L = 50 pF		5.5 7.9	1	9	ns
t_{PHL}					5.5 7.9	1	9	

noise characteristics, V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C (see Note 4)

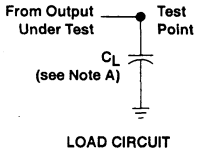
PARAMETER		MIN	TYP	MAX	UNIT
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.4	0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		−0.4	−0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}		4.5		V
$V_{IH(D)}$	High-level dynamic input voltage	2			V
$V_{IL(D)}$	Low-level dynamic input voltage			0.8	V

NOTE 4: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

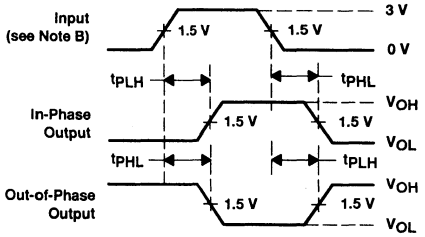
operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance	C_L = 50 pF,	f = 1 MHz	10.5	pF

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



VOLTAGE WAVEFORMS
DELAY TIMES

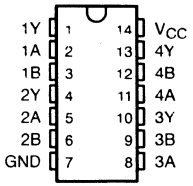
NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

SCLS262A – DECEMBER 1995 – REVISED FEBRUARY 1996

- **Inputs Are TTL-Voltage Compatible**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW) Packages, and Standard Plastic (N) DIPs**

D, DB, N, OR PW PACKAGE
(TOP VIEW)



description

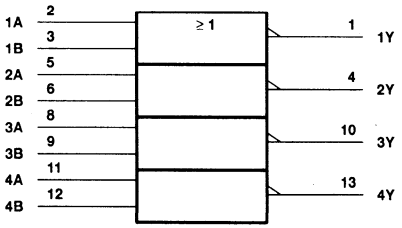
This device contains four independent 2-input NOR gates that perform the Boolean functions $Y = \overline{A} \cdot \overline{B}$ or $Y = \overline{A + B}$ in positive logic.

The SN74AHCT02 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each gate)

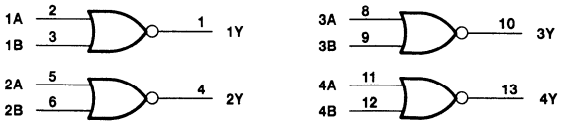
INPUTS		OUTPUT
A	B	Y
H	X	L
X	H	L
L	L	H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



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PRODUCT PREVIEW

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... –0.5 V to 7 V
Output voltage range, V_O (see Note 1) ..... –0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$) ..... –20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... –20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±25 mA
Continuous current through V_{CC} or GND ..... ±50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2): D package ..... 1.25 W
DB or PW package ..... 0.5 W
N package ..... 1.1 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

PRODUCT PREVIEW

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4.5	5.5	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
V_I	Input voltage	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	V
I_{OH}	High-level output current		–8	mA
I_{OL}	Low-level output current		8	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		20	ns/V
T_A	Operating free-air temperature	–40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
V_{OH}	I_{OH} = –50 µA	4.5 V	3.15	3.65		3.15		V
	I_{OH} = –8 mA		2.5			2.4		
V_{OL}	I_{OL} = 50 µA	4.5 V			0.1		0.1	V
	I_{OL} = 8 mA				0.36		0.44	
I_I	$V_I = V_{CC}$ or GND	5.5 V			±0.1		±1	µA
I_{CC}	$V_I = V_{CC}$ or GND, I_O = 0	5.5 V			2		20	µA
ΔI_{CC}‡	One input at 3.4 V, Other inputs at GND or V_{CC}	5.5 V			1.35		1.5	mA
I_{off}	V_O = 5.5 V	0 V			0.5		5	µA
C_i	$V_I = V_{CC}$ or GND	5 V		4	10		10	pF

‡ This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
t_{PLH}	A or B	Y	C_L = 15 pF				1		ns
t_{PHL}							1		
t_{PLH}	A or B	Y	C_L = 50 pF				1		ns
t_{PHL}							1		

noise characteristics, V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C (see Note 4)

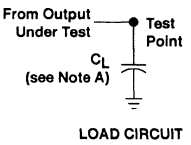
PARAMETER		MIN	TYP	MAX	UNIT
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}			0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}			–0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}				V
$V_{IH(D)}$	High-level dynamic input voltage	2			V
$V_{IL(D)}$	Low-level dynamic input voltage			0.8	V

NOTE 4: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

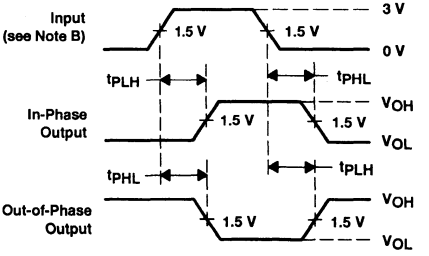
operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	C_L = 50 pF, f = 1 MHz	17	pF

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



VOLTAGE WAVEFORMS
DELAY TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

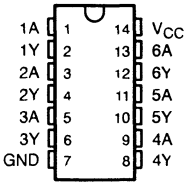
Figure 1. Load Circuit and Voltage Waveforms

PRODUCT PREVIEW

SCLS232A – OCTOBER 1995 – REVISED FEBRUARY 1996

- Inputs Are TTL-Voltage Compatible
- *EPIC*™ (Enhanced-Performance Implanted CMOS) Process
- High Latch-Up Immunity Exceeds 300 mA Per JEDEC Standard JESD-17
- Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW) Packages, and Standard Plastic (N) DIPs

D, DB, N, OR PW PACKAGE
(TOP VIEW)



description

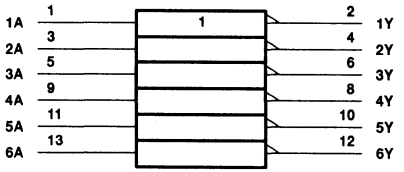
The SN74AHCT04 contains six independent inverters. The device performs the Boolean function $Y = \overline{A}$.

The SN74AHCT04 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each inverter)

INPUT A	OUTPUT Y
H	L
L	H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... –0.5 V to 7 V
Output voltage range, V_O (see Note 1) ..... –0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) ..... –20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±25 mA
Continuous current through V_{CC} or GND ..... ±50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2): D package ..... 1.25 W
DB or PW package ..... 0.5 W
N package ..... 1.1 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4.5	5.5	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
V_I	Input voltage	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	V
I_{OH}	High-level output current		–8	mA
I_{OL}	Low-level output current		8	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		20	ns/V
T_A	Operating free-air temperature	–40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
V_{OH}	I_{OH} = –50 µA		4.5 V	3.15	3.65		3.15		V
	I_{OH} = –8 mA			2.5			2.4		
V_{OL}	I_{OL} = 50 µA		4.5 V			0.1		0.1	V
	I_{OL} = 8 mA					0.36		0.44	
I_I	$V_I = V_{CC}$ or GND		5.5 V			±0.1		±1	µA
I_{CC}	$V_I = V_{CC}$ or GND,	I_O = 0	5.5 V			2		20	µA
ΔI_{CC}‡	One input at 3.4 V,	Other inputs at V_{CC} or GND	5.5 V			1.35		1.5	mA
C_i	$V_I = V_{CC}$ or GND		5 V		4	10		10	pF

‡ This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
t_{PLH}	A	Y	C_L = 15 pF		4.7	6.7	1	7.5	ns
t_{PHL}					4.7	6.7	1	7.5	
t_{PLH}	A	Y	C_L = 50 pF		5.5	7.7	1	8.5	ns
t_{PHL}					5.5	7.7	1	8.5	

noise characteristics, V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C (see Note 4)

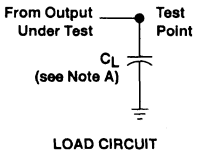
PARAMETER		MIN	TYP	MAX	UNIT
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.8		V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		–0.8		V
$V_{IH(D)}$	High-level dynamic input voltage	2			V
$V_{IL(D)}$	Low-level dynamic input voltage			0.8	V

NOTE 4: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

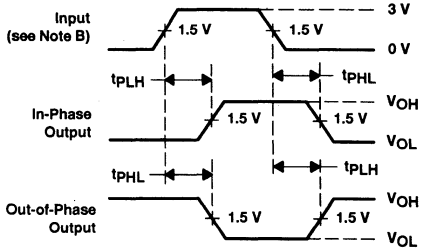
operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	C_L = 50 pF, f = 1 MHz	14	pF

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



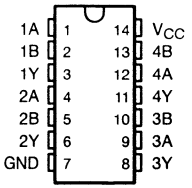
VOLTAGE WAVEFORMS
DELAY TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

- Inputs Are TTL-Voltage Compatible
- *EPIC*™ (Enhanced-Performance Implanted CMOS) Process
- High Latch-Up Immunity Exceeds 300 mA Per JEDEC Standard JESD-17
- Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW) Packages, and Standard Plastic (N) DIPs

D, DB, N, OR PW PACKAGE
(TOP VIEW)



description

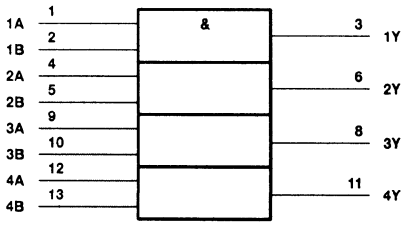
The SN74AHCT08 is a quadruple 2-input positive-AND gate. The device performs the Boolean functions $Y = A \bullet B$ or $Y = \overline{\overline{A} + \overline{B}}$ in positive logic.

The SN74AHCT08 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each gate)

INPUTS		OUTPUT
A	B	Y
H	H	H
L	X	L
X	L	L

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) ..... ± 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ± 20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ± 25 mA
Continuous current through V_{CC} or GND ..... ± 50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2): D package ..... 1.25 W
DB or PW package ..... 0.5 W
N package ..... 1.1 W
Storage temperature range, T_{stg} ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils except for the N package, which has a trace length of zero.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4.5	5.5	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
V_I	Input voltage	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	V
I_{OH}	High-level output current		−8	mA
I_{OL}	Low-level output current		8	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		20	ns/V
T_A	Operating free-air temperature	−40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
V_{OH}	I_{OH} = −50 μA	4.5 V	3.15	3.65		3.15		V
	I_{OH} = −8 mA		2.5			2.4		
V_{OL}	I_{OL} = 50 μA	4.5 V			0.1		0.1	V
	I_{OL} = 8 mA				0.36		0.44	
I_I	$V_I = V_{CC}$ or GND	5.5 V			±0.1		±1	μA
I_{CC}	$V_I = V_{CC}$ or GND, I_O = 0	5.5 V			2		20	μA
ΔI_{CC}‡	One input at 3.4 V, Other inputs at V_{CC} or GND	5.5 V			1.35		1.5	mA
I_{off}	V_O= 5.5 V	0 V			0.5		5	μA
C_i	$V_I = V_{CC}$ or GND	5 V		4	10		10	pF

‡ This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
t_{PLH}	A or B	Y	C_L = 15 pF		5	6.9	1	8	ns
t_{PHL}					5	6.9	1	8	
t_{PLH}	A or B	Y	C_L = 50 pF		5.5	7.9	1	9	ns
t_{PHL}					5.5	7.9	1	9	

noise characteristics, V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C (see Note 4)

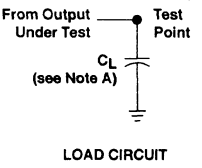
PARAMETER		MIN	TYP	MAX	UNIT
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.4	0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		−0.4	−0.8	V
$V_{IH(D)}$	High-level dynamic input voltage	2			V
$V_{IL(D)}$	Low-level dynamic input voltage			0.8	V

NOTE 4: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

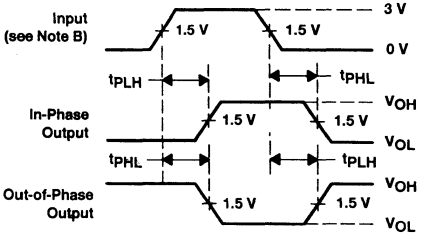
operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	C_L = 50 pF, f = 1 MHz	18	pF

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



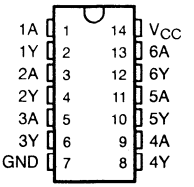
VOLTAGE WAVEFORMS
DELAY TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

- Inputs Are TTL-Voltage Compatible
- *EPIC*™ (Enhanced-Performance Implanted CMOS) Process
- High Latch-Up Immunity Exceeds 300 mA Per JEDEC Standard JESD-17
- Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW) Packages, and Standard Plastic (N) DIPs

D, DB, N, OR PW PACKAGE
(TOP VIEW)



description

The SN74AHCT14 contains six independent inverters. The device performs the Boolean function $Y = \overline{A}$.

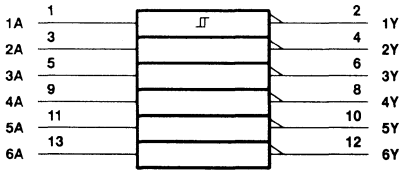
Each circuit functions as an independent inverter, but because of the Schmitt action, the inverters have different input threshold levels for positive- (V_{T+}) and for negative-going (V_{T-}) signals.

The SN74AHCT14 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE
(each inverter)

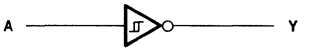
INPUT A	OUTPUT Y
H	L
L	H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) ..... − 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... − 20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ± 25 mA
Continuous current through V_{CC} or GND ..... ± 50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2): D package ..... 1.25 W
DB or PW package ..... 0.5 W
N package ..... 1.1 W
Storage temperature range, T_{stg} ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4.5	5.5	V
V_{IH}	High-level input voltage	2.1		V
V_{IL}	Low-level input voltage		0.5	V
V_I	Input voltage	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	V
I_{OH}	High-level output current		−8	mA
I_{OL}	Low-level output current		8	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		20	ns/V
T_A	Operating free-air temperature	− 40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C					UNIT
			MIN	TYP	MAX	MIN	MAX	
V_{T+} Positive-going input threshold voltage		4.5 V			2		2	V
		5.5 V			2		2	
V_{T-} Negative-going input threshold voltage		4.5 V	0.6			0.6		V
		5.5 V	0.6			0.6		
ΔV_T Hysteresis ($V_{T+} - V_{T-}$)		4.5 V	0.4		1.4	0.4	1.4	V
		5.5 V	0.5		1.6	0.5	1.6	
V_{OH}	I_{OH} = – 50 μA	4.5 V	3.15	3.65		3.15		V
	I_{OH} = – 8 mA	4.5 V	2.5			2.4		
V_{OL}	I_{OL} = 50 μA	4.5 V			0.1		0.1	V
	I_{OL} = 8 mA	4.5 V			0.36		0.44	
I_I	$V_I = V_{CC}$ or GND	5.5 V			± 0.1		± 1	μA
I_{CC}	$V_I = V_{CC}$ or GND, I_O = 0	5.5 V			2		20	μA
C_i	$V_I = V_{CC}$ or GND	5 V		2	10		10	pF

switching characteristics over recommended operating free-air temperature range V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C					UNIT
				MIN	TYP	MAX	MIN	MAX	
t_{PLH}	A	Y	C_L = 15 pF		4	7	1	8	ns
t_{PHL}					4	7	1	8	
t_{PLH}	A	Y	C_L = 50 pF		5.5	8	1	9	ns
t_{PHL}					5.5	8	1	9	

noise characteristics, V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C (see Note 4)

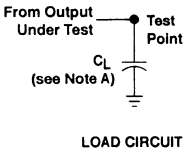
PARAMETER		MIN	TYP	MAX	UNIT
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.9		V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		–0.7		V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}		4.3		V
$V_{IH(D)}$	High-level dynamic input voltage	2.1			V
$V_{IL(D)}$	Low-level dynamic input voltage			0.5	V

NOTE 4: Characteristics are determined during product characterization and ensured by design and for surface-mount packages only.

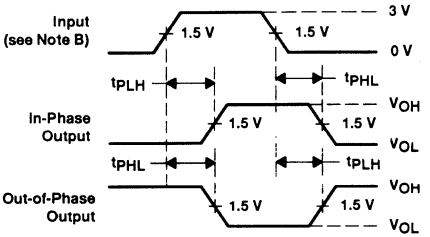
operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	C_L = 50 pF, f = 1 MHz	12	pF

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



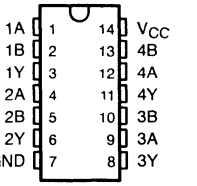
VOLTAGE WAVEFORMS
DELAY TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

- **Inputs Are TTL-Voltage Compatible**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **High Latch-Up Immunity Exceeds 300 mA Per JEDEC Standard JESD-17**
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW) Packages, and Standard Plastic (N) DIPs**

D, DB, N, OR PW PACKAGE
(TOP VIEW)



description

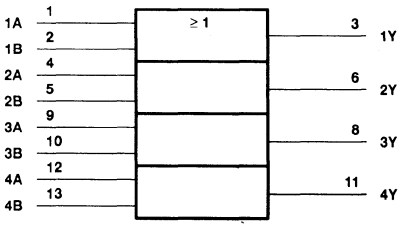
The SN74AHCT32 is a quadruple 2-input positive-OR gate. The device performs the Boolean functions $Y = \overline{A \bullet B}$ or $Y = A + B$ in positive logic.

The SN74AHCT32 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each gate)

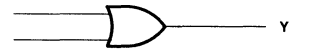
INPUTS		OUTPUT
A	B	Y
H	X	H
X	H	H
L	L	L

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) ..... ± 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ± 20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ± 25 mA
Continuous current through V_{CC} or GND ..... ± 50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2): D package ..... 1.25 W
DB or PW package ..... 0.5 W
N package ..... 1.1 W
Storage temperature range, T_{stg} ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4.5	5.5	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
V_I	Input voltage	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	V
I_{OH}	High-level output current		−8	mA
I_{OL}	Low-level output current		8	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		20	ns/V
T_A	Operating free-air temperature	−40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
V_{OH}	I_{OH} = −50 μA		4.5 V	3.15	3.65		3.15		V
	I_{OH} = −8 mA			2.5			2.4		
V_{OL}	I_{OL} = 50 μA		4.5 V			0.1		0.1	V
	I_{OL} = 8 mA					0.36		0.44	
I_I	$V_I = V_{CC}$ or GND		5.5 V			±0.1		±1	μA
I_{CC}	$V_I = V_{CC}$ or GND,	I_O = 0	5.5 V			2		20	μA
ΔI_{CC}‡	One input at 3.4 V,	Other inputs at V_{CC} or GND	5.5 V			1.35		1.5	mA
I_{off}	V_O = 5.5 V		0 V			0.5		5	μA
C_i	$V_I = V_{CC}$ or GND		5 V		2	10		10	pF

‡ This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
t_{PLH}	A or B	Y	C_L = 15 pF		5	6.9	1	8	ns
t_{PHL}					5	6.9	1	8	
t_{PLH}	A or B	Y	C_L = 50 pF		5.5	7.9	1	9	ns
t_{PHL}					5.5	7.9	1	9	

noise characteristics, V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C (see Note 4)

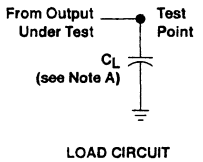
PARAMETER		MIN	TYP	MAX	UNIT
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.4	0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		−0.4	−0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}		4.1		V
$V_{IH(D)}$	High-level dynamic input voltage	2			V
$V_{IL(D)}$	Low-level dynamic input voltage			0.8	V

NOTE 4: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

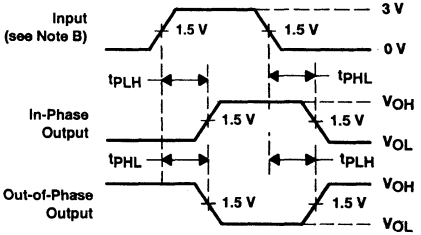
operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	C_L = 50 pF, f = 1 MHz	11.5	pF

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



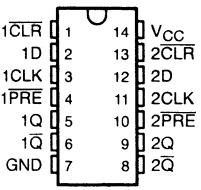
VOLTAGE WAVEFORMS
DELAY TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

- **Inputs Are TTL-Voltage Compatible**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW) Packages, and Standard Plastic (N) DIPs**

D, DB, N, OR PW PACKAGE
(TOP VIEW)



description

The SN74AHCT74 is a dual positive-edge-triggered D-type flip-flop.

A low level at the preset ($\overline{PRE}$) or clear ($\overline{CLR}$) inputs sets or resets the outputs regardless of the levels of the other inputs. When $\overline{PRE}$ and $\overline{CLR}$ are inactive (high), data at the data (D) input meeting the setup time requirements is transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold-time interval, data at the D input can be changed without affecting the levels at the outputs.

The SN74AHCT74 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE

INPUTS				OUTPUTS	
$\overline{PRE}$	$\overline{CLR}$	CLK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H†	H†
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$

† This configuration is nonstable; that is, it does not persist when $\overline{PRE}$ or $\overline{CLR}$ returns to its inactive (high) level.

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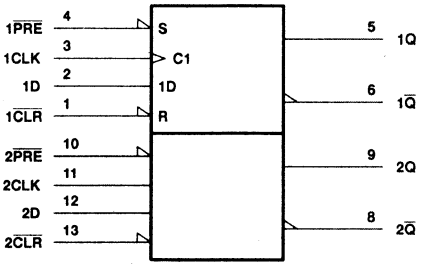
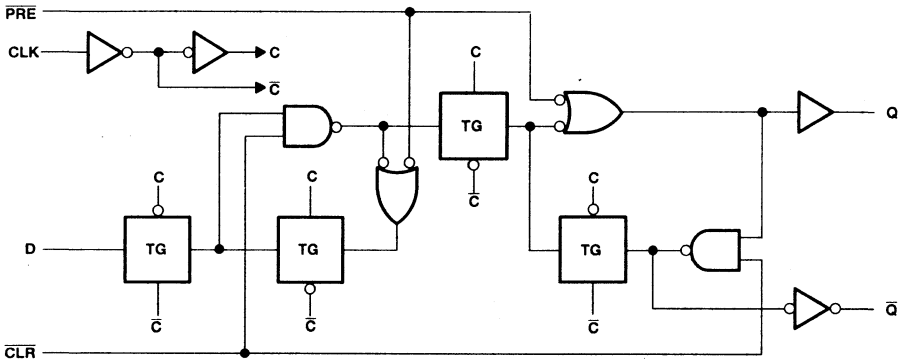
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram, each flip-flop (positive logic)



PRODUCT PREVIEW

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... –0.5 V to 7 V
Output voltage range, V_O (see Note 1) ..... –0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) ..... –20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... –20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) ..... ±25 mA
Continuous current through V_{CC} or GND ..... ±50 mA
Maximum power dissipation at $T_A = 55°C$ (in still air) (see Note 2): D package ..... 1.25 W
DB or PW package ..... 0.5 W
N package ..... 1.1 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4.5	5.5	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
V_I	Input voltage	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	V
I_{OH}	High-level output current		–8	mA
I_{OL}	Low-level output current		8	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		20	ns/V
T_A	Operating free-air temperature	–40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	$T_A = 25°C$			MIN	MAX	UNIT
				MIN	TYP	MAX			
V_{OH}	$I_{OH} = –50\ \mu A$		4.5 V	3.15	3.65		3.15		V
	$I_{OH} = –8$ mA			2.5			2.4		
V_{OL}	$I_{OL} = 50\ \mu A$		4.5 V			0.1		0.1	V
	$I_{OL} = 8$ mA					0.36		0.44	
I_I	$V_I = V_{CC}$ or GND		5.5 V			±0.1		±1	µA
I_{CC}	$V_I = V_{CC}$ or GND,	$I_O = 0$	5.5 V			2		20	µA
ΔI_{CC}‡	One input at 3.4 V,	Other inputs at GND or V_{CC}	5.5 V			1.35		1.5	mA
I_{off}	$V_O = 5.5$ V		0 V			0.5		5	µA
C_i	$V_I = V_{CC}$ or GND		5 V		4	10		10	pF

‡ This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

PRODUCT PREVIEW

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

PARAMETER			T_A = 25°C		MIN	MAX	UNIT
			MIN	MAX			
t_w	Pulse duration	$\overline{PRE}$ or $\overline{CLR}$ low	5		5		ns
		CLK	5		5		
t_{su}	Setup time before CLK↑	Data	5		5		ns
		$\overline{PRE}$ or $\overline{CLR}$ inactive	5		5		
t_h	Hold time, data after CLK↑		0		0		ns
t_{rem}	Minimum removal time		3.5		3.5		ns

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
f_{max}			C_L = 15 pF	100	160		80		MHz
			C_L = 50 pF	80	140		65		
t_{PLH}	PRE or CLR	Q or $\overline{Q}$	C_L = 15 pF		7.6	10.4	1	12	ns
t_{PHL}					7.6	10.4	1	12	
t_{PLH}	CLK	Q or $\overline{Q}$	C_L = 15 pF		5.8	7.8	1	9	ns
t_{PHL}					5.8	7.8	1	9	
t_{PLH}	$\overline{PRE}$ or $\overline{CLR}$	Q or $\overline{Q}$	C_L = 50 pF		8.1	11.4	1	13	ns
t_{PHL}					8.1	11.4	1	13	
t_{PLH}	CLK	Q or $\overline{Q}$	C_L = 50 pF		6.3	8.8	1	10	ns
t_{PHL}					6.3	8.8	1	10	

noise characteristics, V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C (see Note 4)

PARAMETER		MIN	TYP	MAX	UNIT
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}			0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}			–0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}				V
$V_{IH(D)}$	High-level dynamic input voltage	2			V
$V_{IL(D)}$	Low-level dynamic input voltage			0.8	V

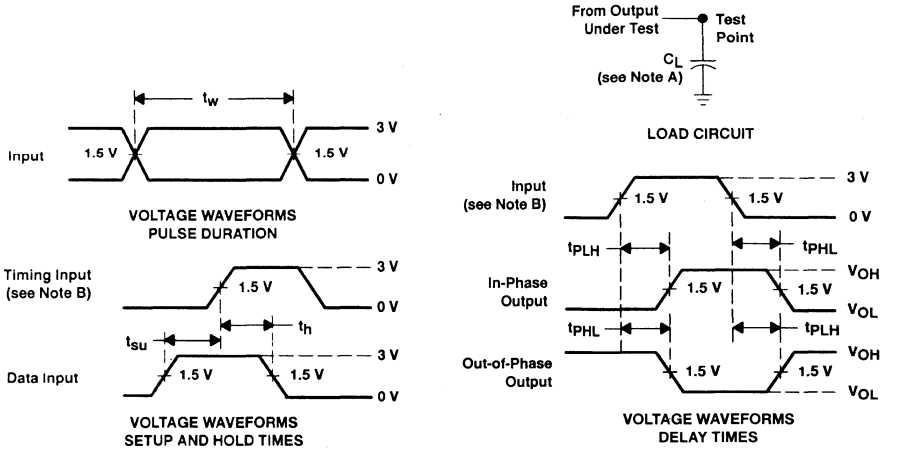
NOTE 4: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	C_L = 50 pF, f = 1 MHz	24	pF

PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

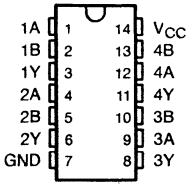
Figure 1. Load Circuit and Voltage Waveforms

PRODUCT PREVIEW

SCLS250A – OCTOBER 1995 – REVISED FEBRUARY 1996

- Inputs Are TTL-Voltage Compatible
- *EPIC*™ (Enhanced-Performance Implanted CMOS) Process
- High Latch-Up Immunity Exceeds 300 mA Per JEDEC Standard JESD-17
- Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW) Packages, and Standard Plastic (N) DIPs

D, DB, N, OR PW PACKAGE
(TOP VIEW)



description

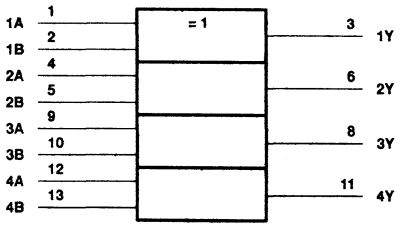
The SN74AHCT86 is a quadruple 2-input exclusive-OR gate. The device performs the Boolean functions $Y = A \oplus B$ or $Y = \overline{A}B + A\overline{B}$ in positive logic.

The SN74AHCT86 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each gate)

INPUTS		OUTPUT
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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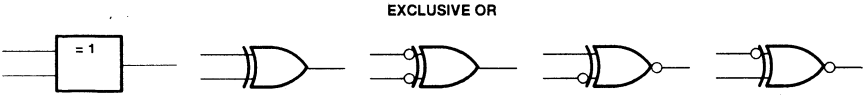
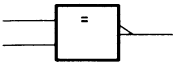
exclusive-OR logic

An exclusive-OR gate has many applications, some of which can be represented better by alternative logic symbols.



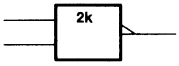
These are five equivalent exclusive-OR symbols valid for an SN74AHCT86 gate in positive logic: negation may be shown at any two ports.

LOGIC-IDENTITY ELEMENT



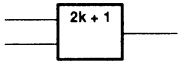
The output is active (low) if all inputs stand at the same logic level (i.e., A = B).

EVEN-PARITY ELEMENT



The output is active (low) if an even number of inputs (i.e., 0 or 2) are active.

ODD-PARITY ELEMENT



The output is active (high) if an odd number of inputs (i.e., only 1 of the 2) are active.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) ..... − 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... − 20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) ..... ± 25 mA
Continuous current through V_{CC} or GND ..... ± 50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2): D package ..... 1.25 W
DB or PW package ..... 0.5 W
N package ..... 1.1 W
Storage temperature range, T_{stg} ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4.5	5.5	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
V_I	Input voltage	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	V
I_{OH}	High-level output current		−8	mA
I_{OL}	Low-level output current		8	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		20	ns/V
T_A	Operating free-air temperature	−40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
V_{OH}	I_{OH} = − 50 μA		4.5 V	3.15	3.65		3.15		V
	I_{OH} = − 8 mA			2.5			2.4		
V_{OL}	I_{OL} = 50 μA		4.5 V			0.1		0.1	V
	I_{OL} = 8 mA					0.36		0.44	
I_I	$V_I = V_{CC}$ or GND		5.5 V			±0.1		±1	μA
I_{CC}	$V_I = V_{CC}$ or GND,	I_O = 0	5.5 V			2		20	μA
ΔI_{CC}†	One input at 3.4 V,	Other inputs at V_{CC} or GND	5.5 V			1.35		1.5	mA
I_{off}	V_O = 5.5 V		0 V			0.5		5	μA
C_i	$V_I = V_{CC}$ or GND		5 V		4	10		10	pF

† This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
t_{PLH}	A or B	Y	C_L = 15 pF		5	6.9	1	8	ns
t_{PHL}					5	6.9	1	8	
t_{PLH}	A or B	Y	C_L = 50 pF		5.5	7.9	1	9	ns
t_{PHL}					5.5	7.9	1	9	

noise characteristics, V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C (see Note 4)

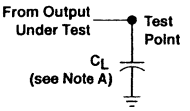
PARAMETER		MIN	TYP	MAX	UNIT
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.4	0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		−0.4	−0.8	V
$V_{IH(D)}$	High-level dynamic input voltage	2			V
$V_{IL(D)}$	Low-level dynamic input voltage			0.8	V

NOTE 4: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

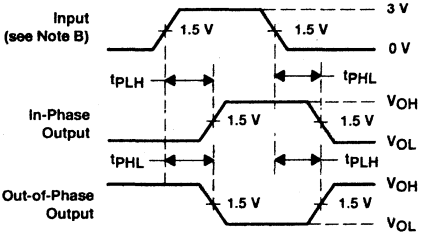
operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	C_L = 50 pF, f = 1 MHz	18	pF

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



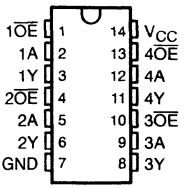
VOLTAGE WAVEFORMS
DELAY TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

- Inputs Are TTL-Voltage Compatible
- *EPIC*™ (Enhanced-Performance Implanted CMOS) Process
- Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW) Packages, and Standard Plastic (N) DIPs

D, DB, N, OR PW PACKAGE
(TOP VIEW)



description

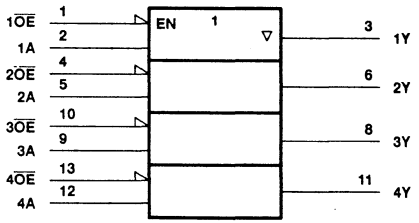
The SN74AHCT125 quadruple bus buffer gate features independent line drivers with 3-state outputs. Each output is disabled when the associated output-enable ($\overline{OE}$) input is high. When $\overline{OE}$ is low, the respective gate passes the data from the A input to its Y output.

The SN74AHCT125 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each buffer)

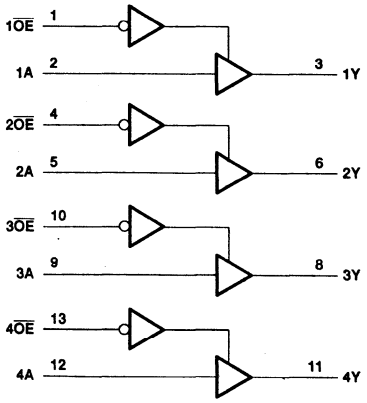
INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	H
L	L	L
H	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$) ..... − 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... − 20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ± 25 mA
Continuous current through V_{CC} or GND ..... ± 50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2): D package ..... 1.25 W
DB or PW package ..... 0.5 W
N package ..... 1.1 W
Storage temperature range, T_{stg} ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

PRODUCT PREVIEW

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4.5	5.5	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
V_I	Input voltage	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	V
I_{OH}	High-level output current		−8	mA
I_{OL}	Low-level output current		8	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		20	ns/V
T_A	Operating free-air temperature	−40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
V_{OH}		I_{OH} = − 50 μA	4.5 V	3.15	3.65		3.15		V
		I_{OH} = − 8 mA		2.5			2.4		
V_{OL}		I_{OL} = 50 μA	4.5 V			0.1		0.1	V
		I_{OL} = 8 mA				0.36		0.44	
I_I	A or $\overline{OE}$ inputs	$V_I = V_{CC}$ or GND	5.5 V			± 0.1		± 1	μA
I_{OZ}		$V_I = V_{CC}$ or GND	5.5 V			± 0.25		± 2.5	μA
I_{CC}		$V_I = V_{CC}$ or GND, I_O = 0	5.5 V			2		20	μA
ΔI_{CC}‡		One input at 3.4 V, Other inputs at V_{CC} or GND	5.5 V			1.35		1.5	mA
C_i		$V_I = V_{CC}$ or GND	5 V		4	10		10	pF
C_o		$V_O = V_{CC}$ or GND	5 V		15				pF

‡ This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
t_{PLH}	A	Y	C_L = 15 pF						ns
t_{PHL}									
t_{PZH}	$\overline{OE}$	Y							ns
t_{PZL}									
t_{PHZ}	$\overline{OE}$	Y							ns
t_{PLZ}									
t_{PLH}	A	Y	C_L = 50 pF						ns
t_{PHL}									
t_{PZH}	$\overline{OE}$	Y							ns
t_{PZL}									
t_{PHZ}	$\overline{OE}$	Y							ns
t_{PLZ}									

output-skew characteristics, C_L = 50 pF (see Note 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
$t_{sk(o)}$	A	Y	5 V ± 0.5 V			1		1	ns

NOTE 4: Characteristics are determined during product characterization and ensured by design.

noise characteristics, V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C (see Note 5)

PARAMETER		MIN	TYP	MAX	UNIT
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}			0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}			−0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}				V
$V_{IH(D)}$	High-level dynamic input voltage	2			V
$V_{IL(D)}$	Low-level dynamic input voltage			0.8	V

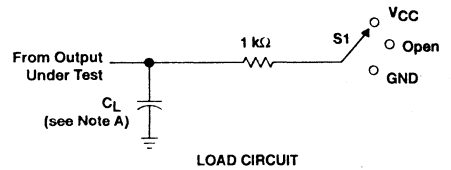
NOTE 5: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
C_{pd}	Power dissipation capacitance	C_L = 50 pF,	f = 1 MHz				pF

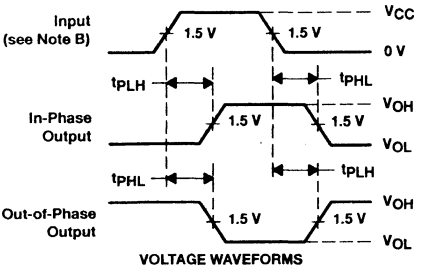
PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

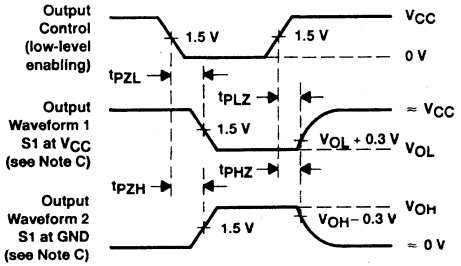


LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND



VOLTAGE WAVEFORMS
DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

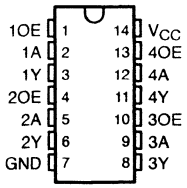
NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PRODUCT PREVIEW

- Inputs Are TTL-Voltage Compatible
- *EPIC*™ (Enhanced-Performance Implanted CMOS) Process
- Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW) Packages, and Standard Plastic (N) DIPs

D, DB, N, OR PW PACKAGE
(TOP VIEW)



description

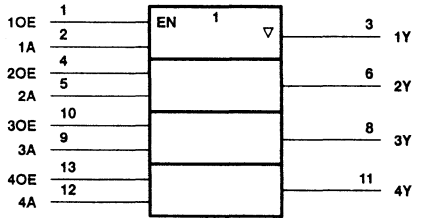
The SN74AHCT126 quadruple bus buffer gate features independent line drivers with 3-state outputs. Each output is disabled when the associated output-enable (OE) input is low. When OE is high, the respective gate passes the data from the A input to its Y output.

The SN74AHCT126 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE
(each buffer)

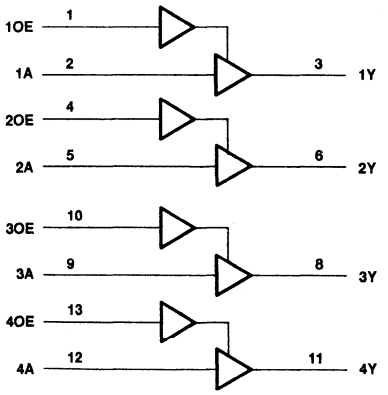
INPUTS		OUTPUT
OE	A	Y
H	H	H
H	L	L
L	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$) ..... − 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... − 20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ± 25 mA
Continuous current through V_{CC} or GND ..... ± 50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2): D package ..... 1.25 W
DB or PW package ..... 0.5 W
N package ..... 1.1 W
Storage temperature range, T_{stg} ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

PRODUCT PREVIEW

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4.5	5.5	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
V_I	Input voltage	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	V
I_{OH}	High-level output current		−8	mA
I_{OL}	Low-level output current		8	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		20	ns/V
T_A	Operating free-air temperature	− 40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
V_{OH}		I_{OH} = − 50 μA	4.5 V	3.15	3.65		3.15		V
		I_{OH} = − 8 mA		2.5			2.4		
V_{OL}		I_{OL} = 50 μA	4.5 V			0.1		0.1	V
		I_{OL} = 8 mA				0.36		0.44	
I_I	A or OE inputs	$V_I = V_{CC}$ or GND	5.5 V			± 0.1		± 1	μA
I_{OZ}		$V_I = V_{CC}$ or GND	5.5 V			± 0.25		± 2.5	μA
I_{CC}		$V_I = V_{CC}$ or GND, I_O = 0	5.5 V			2		20	μA
ΔI_{CC}‡		One input at 3.4 V, Other inputs at V_{CC} or GND	5.5 V			1.35		1.5	mA
C_i		$V_I = V_{CC}$ or GND	5 V		4	10		10	pF
C_o		$V_O = V_{CC}$ or GND	5 V		15				pF

‡ This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
t_{PLH}	A	Y	C_L = 15 pF						ns
t_{PHL}									
t_{PZH}	OE	Y							ns
t_{PZL}									
t_{PHZ}	OE	Y							ns
t_{PLZ}									
t_{PLH}	A	Y	C_L = 50 pF						ns
t_{PHL}									
t_{PZH}	OE	Y							ns
t_{PZL}									
t_{PHZ}	OE	Y							ns
t_{PLZ}									

output-skew characteristics, C_L = 50 pF (see Note 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
$t_{sk(o)}$	A	Y	5 V ± 0.5 V			1		1	ns

NOTE 4: Characteristics are determined during product characterization and ensured by design.

noise characteristics, V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C (see Note 5)

	PARAMETER	MIN	TYP	MAX	UNIT
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}			0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}			−0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}				V
$V_{IH(D)}$	High-level dynamic input voltage	2			V
$V_{IL(D)}$	Low-level dynamic input voltage			0.8	V

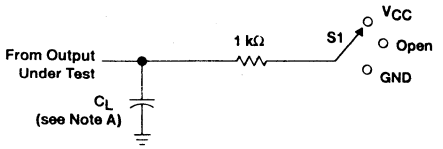
NOTE 5: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

operating characteristics, V_{CC} = 5 V, T_A = 25°C

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_{pd}	Power dissipation capacitance	C_L = 50 pF, f = 1 MHz				pF

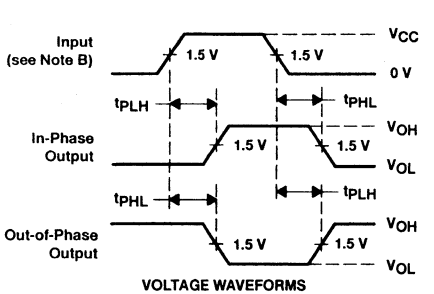
PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

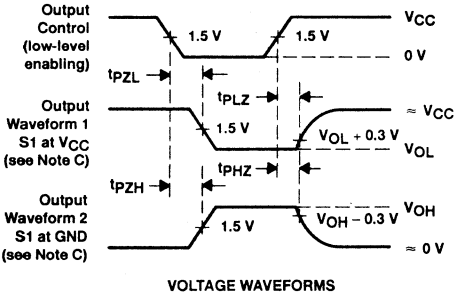


LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND



VOLTAGE WAVEFORMS
DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

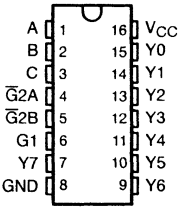
NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PRODUCT PREVIEW

- **Inputs Are TTL-Voltage Compatible**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **Designed Specifically for High-Speed Memory Decoders and Data Transmission Systems**
- **Incorporates Three Enable Inputs to Simplify Cascading and/or Data Reception**
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW) Packages, and Standard Plastic (N) DIPs**

D, DB, N, OR PW PACKAGE
(TOP VIEW)



description

The SN74AHCT138 3-line to 8-line decoder/demultiplexer is designed to be used in high-performance memory-decoding or data-routing applications requiring very short propagation delay times. In high-performance memory systems, this decoder can be used to minimize the effects of system decoding. When employed with high-speed memories utilizing a fast enable circuit, the delay times of this decoder and the enable time of the memory are usually less than the typical access time of the memory. This means that the effective system delay introduced by the decoder is negligible.

The conditions at the binary-select inputs and the three enable inputs select one of eight input lines. Two active-low and one active-high enable inputs reduce the need for external gates or inverters when expanding. A 24-line decoder can be implemented without external inverters and a 32-line decoder requires only one inverter. An enable input can be used as a data input for demultiplexing applications.

The SN74AHCT138 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE

ENABLE INPUTS			SELECT INPUTS			OUTPUTS							
G1	$\overline{G2A}$	$\overline{G2B}$	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	L	H	H	H	H	H	L	H	H	H	H
H	L	L	H	L	L	H	H	H	H	L	H	H	H
H	L	L	H	L	H	H	H	H	H	H	L	H	H
H	L	L	H	H	L	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L

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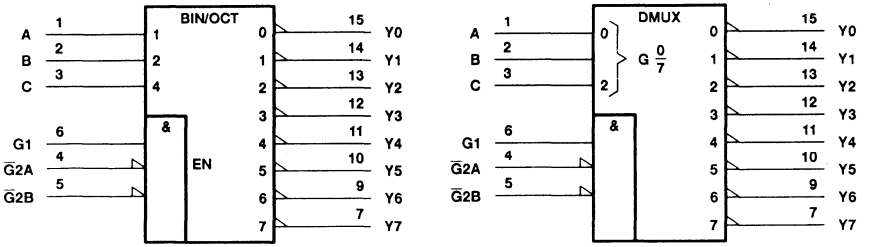
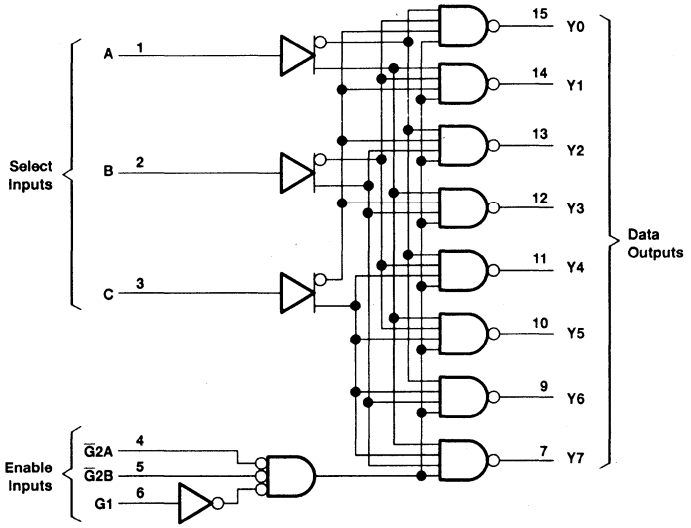
logic symbols (alternatives)†



† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



PRODUCT PREVIEW

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... –0.5 V to 7 V
Output voltage range, V_O (see Note 1) ..... –0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$) ..... –20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... –20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) ..... ±25 mA
Continuous current through V_{CC} or GND ..... ±75 mA
Maximum power dissipation at $T_A = 55°C$ (in still air) (see Note 2): D package ..... 1.3 W
DB package ..... 0.55 W
N package ..... 1.1 W
PW package ..... 0.5 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4.5	5.5	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
V_I	Input voltage	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	V
I_{OH}	High-level output current		–8	mA
I_{OL}	Low-level output current		8	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		20	ns/V
T_A	Operating free-air temperature	–40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	$T_A = 25°C$			MIN	MAX	UNIT
				MIN	TYP	MAX			
V_{OH}	$I_{OH} = –50\ \mu A$		4.5 V	3.15	3.65		3.15		V
	$I_{OH} = –8$ mA			2.5			2.4		
V_{OL}	$I_{OL} = 50\ \mu A$		4.5 V			0.1		0.1	V
	$I_{OL} = 8$ mA					0.36		0.44	
I_I	$V_I = V_{CC}$ or GND		5.5 V			±0.1		±1	µA
I_{CC}	$V_I = V_{CC}$ or GND,	$I_O = 0$	5.5 V			4		40	µA
ΔI_{CC}‡	One input at 3.4 V,	Other inputs at V_{CC} or GND	5.5 V			1.35		1.5	mA
I_{off}	$V_O = 5.5$ V		0 V			0.5		5	µA
C_i	$V_I = V_{CC}$ or GND		5 V		4	10		10	pF

‡ This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

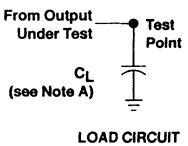
PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
t_{PLH}	A, B, C	Any Y	C_L = 15 pF		7.6	10.4	1	12	ns
t_{PHL}					7.6	10.4	1	12	
t_{PLH}	G1	Any Y	C_L = 15 pF		6.6	9.1	1	10.5	ns
t_{PHL}					6.6	9.1	1	10.5	
t_{PLH}	$\overline{G}$2A, $\overline{G}$2B	Any Y	C_L = 15 pF		7	9.6	1	11	ns
t_{PHL}					7	9.6	1	11	
t_{PLH}	A, B, C	Any Y	C_L = 50 pF		8.1	11.4	1	13	ns
t_{PHL}					8.1	11.4	1	13	
t_{PLH}	G1	Any Y	C_L = 50 pF		7.1	10.1	1	11.5	ns
t_{PHL}					7.1	10.1	1	11.5	
t_{PLH}	$\overline{G}$2A, $\overline{G}$2B	Any Y	C_L = 50 pF		7.5	10.6	1	12	ns
t_{PHL}					7.5	10.6	1	12	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

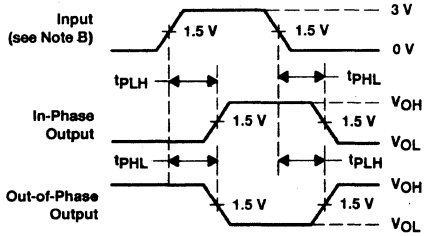
PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per gate	C_L = 50 pF, f = 1 MHz	49	pF

PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



VOLTAGE WAVEFORMS
DELAY TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

APPLICATION INFORMATION

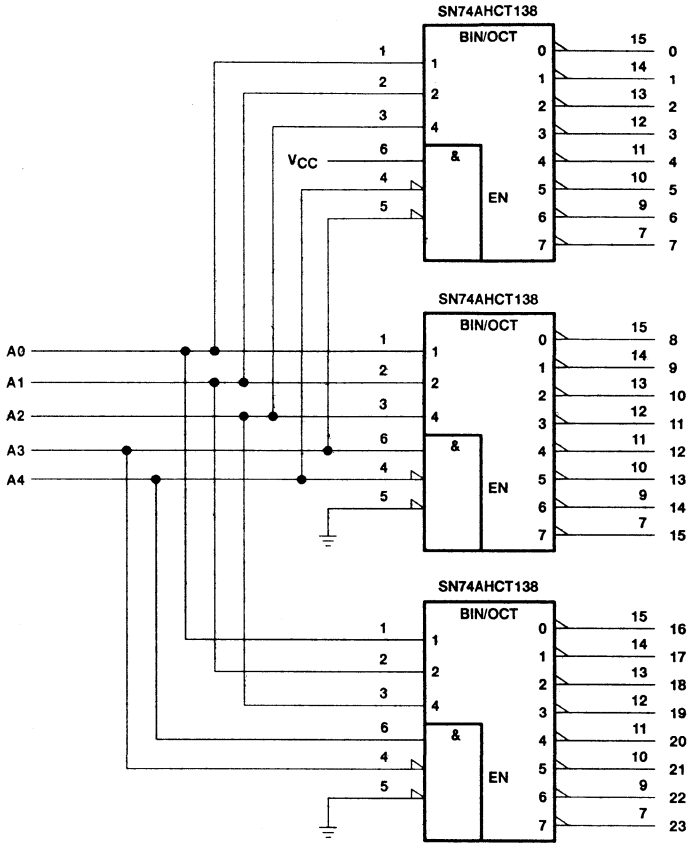


Figure 2. 24-Bit Decoding Scheme

PRODUCT PREVIEW

APPLICATION INFORMATION

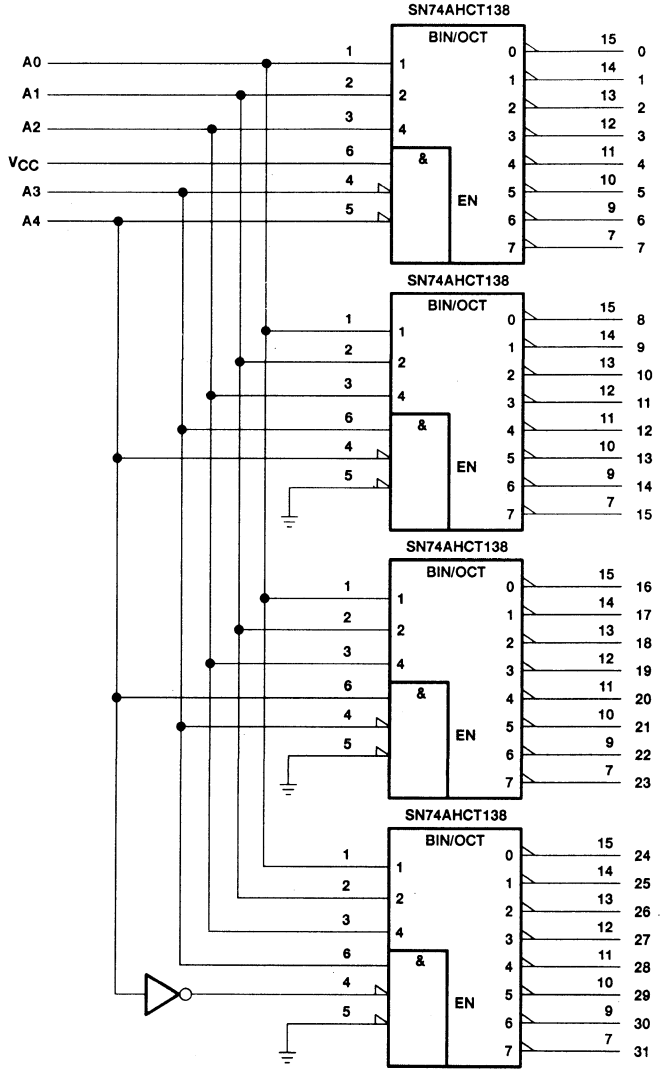


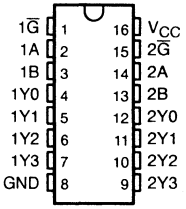
Figure 3. 32-Bit Decoding Scheme

PRODUCT PREVIEW

SCLS267A – DECEMBER 1995 – REVISED FEBRUARY 1996

- Inputs Are TTL-Voltage Compatible
- *EPIC*™ (Enhanced-Performance Implanted CMOS) Process
- Designed Specifically for High-Speed Memory Decoders and Data Transmission Systems
- Incorporates Two Enable Inputs to Simplify Cascading and/or Data Reception
- Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW) Packages, and Standard Plastic (N) DIPs

D, DB, N, OR PW PACKAGE
(TOP VIEW)



description

The SN74AHCT139 is a dual 2-line to 4-line decoder/demultiplexer designed for 2-V to 5.5-V V_{CC} operation. This device is designed to be used in high-performance memory-decoding or data-routing applications requiring very short propagation delay times. In high-performance memory systems, this decoder can be used to minimize the effects of system decoding. When used with high-speed memories utilizing a fast enable circuit, the delay times of this decoder and the enable time of the memory are usually less than the typical access time of the memory. This means that the effective system delay introduced by the decoder is negligible.

The active-low enable ($\overline{G}$) input can be used as a data line in demultiplexing applications. These decoders/demultiplexers feature fully buffered inputs, each of which represents only one normalized load to its driving circuit.

The SN74AHCT139 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE

INPUTS			OUTPUTS			
$\overline{G}$	SELECT					
	B	A	Y0	Y1	Y2	Y3
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L

PRODUCT PREVIEW

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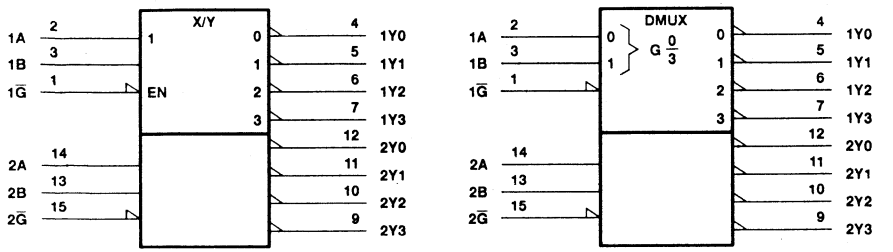
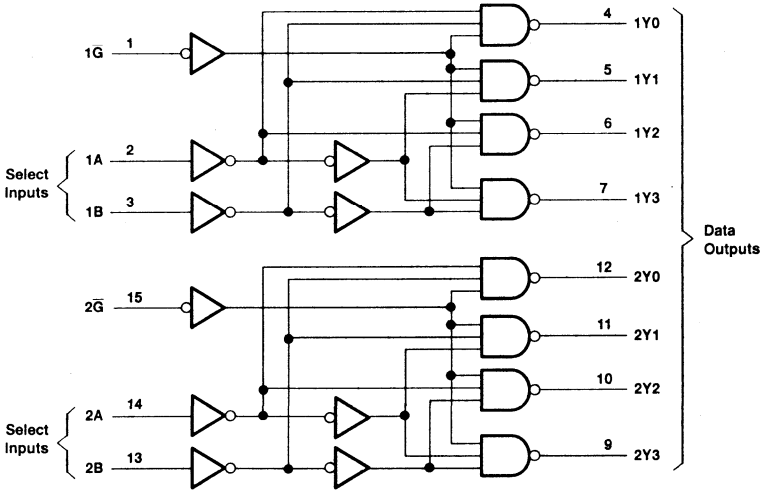
logic symbols (alternatives)†



† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12

logic diagram (positive logic)



PRODUCT PREVIEW

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... –0.5 V to 7 V
Output voltage range, V_O (see Note 1) ..... –0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$) ..... –20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... –20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) ..... ±25 mA
Continuous current through V_{CC} or GND ..... ±75 mA
Maximum power dissipation at $T_A = 55°C$ (in still air) (see Note 2): D package ..... 1.3 W
DB package ..... 0.55 W
N package ..... 1.1 W
PW package ..... 0.5 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4.5	5.5	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
V_I	Input voltage	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	V
I_{OH}	High-level output current		–8	mA
I_{OL}	Low-level output current		8	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		20	ns/V
T_A	Operating free-air temperature	–40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	$T_A = 25°C$			MIN	MAX	UNIT
				MIN	TYP	MAX			
V_{OH}	$I_{OH} = -50\ \mu A$		4.5 V	3.15	3.65		3.15		V
	$I_{OH} = -8$ mA			2.5			2.4		
V_{OL}	$I_{OL} = 50\ \mu A$		4.5 V			0.1		0.1	V
	$I_{OL} = 8$ mA					0.36		0.44	
I_I	$V_I = V_{CC}$ or GND		5.5 V			±0.1		±1	μA
I_{CC}	$V_I = V_{CC}$ or GND,	$I_O = 0$	5.5 V			2		20	μA
ΔI_{CC}‡	One input at 3.4 V,	Other inputs at V_{CC} or GND	5.5 V			1.35		1.5	mA
C_i	$V_I = V_{CC}$ or GND		5 V		4.5				pF

‡ This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

PRODUCT PREVIEW

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

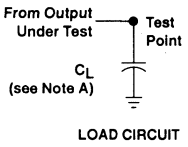
PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
t_{PLH}	A or B	Y	C_L = 15 pF				1		ns
t_{PHL}							1		
t_{PLH}	$\overline{G}$	Y	C_L = 15 pF				1		ns
t_{PHL}							1		
t_{PLH}	A or B	Y	C_L = 50 pF				1		ns
t_{PHL}							1		
t_{PLH}	$\overline{G}$	Y	C_L = 50 pF				1		ns
t_{PHL}							1		

operating characteristics, V_{CC} = 5 V, T_A = 25°C

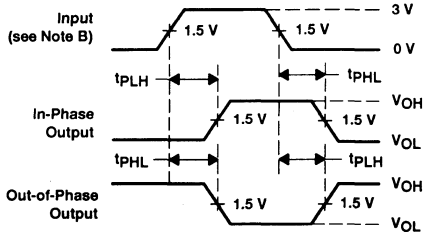
PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	C_L = 50 pF, f = 1 MHz	26	pF

PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



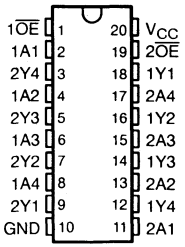
VOLTAGE WAVEFORMS
DELAY TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

- **Inputs Are TTL-Voltage Compatible**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **High Latch-Up Immunity Exceeds 300 mA Per JEDEC Standard JESD-17**
- **Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW) Packages, and Standard Plastic (N) DIPs**

DB, DW, N, OR PW PACKAGE
(TOP VIEW)



description

This octal buffer/driver is designed specifically to improve both the performance and density of 3-state memory-address drivers, clock drivers, and bus-oriented receivers and transmitters.

The SN74AHCT240 is organized as two 4-bit buffers/line drivers with separate output-enable ($\overline{OE}$) inputs. When $\overline{OE}$ is low, the device passes data from the A inputs to the Y outputs. When $\overline{OE}$ is high, the outputs are in the high-impedance state.

The SN74AHCT240 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each buffer)

INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	L
L	L	H
H	X	Z

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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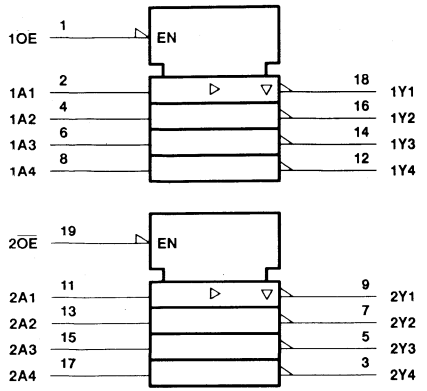
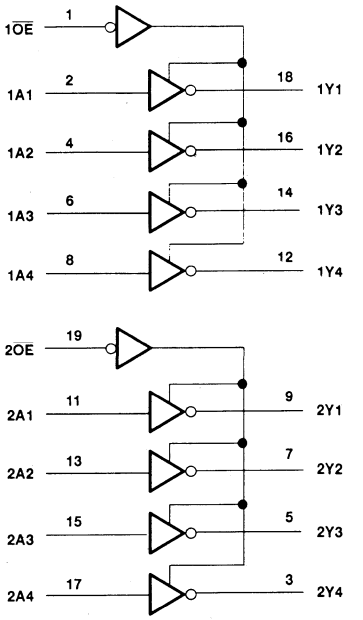
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC}	−0.5 V to 7 V
Input voltage range, V_I (see Note 1)	−0.5 V to 7 V
Output voltage range, V_O (see Note 1)	−0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	± 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	± 20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	± 25 mA
Continuous current through V_{CC} or GND	± 75 mA
Maximum power dissipation at $T_A = 55°C$ (in still air) (see Note 2): DB package	0.6 W
DW package	1.6 W
N package	1.3 W
PW package	0.7 W
Storage temperature range, T_{stg}	−65°C to 150°C

‡Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4.5	5.5	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
V_I	Input voltage	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	V
I_{OH}	High-level output current		−8	mA
I_{OL}	Low-level output current		8	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		20	ns/V
T_A	Operating free-air temperature	− 40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
V_{OH}	I_{OH} = − 50 μA		4.5 V	3.15	3.65		3.15		V
	I_{OH} = − 8 mA			2.5			2.4		
V_{OL}	I_{OL} = 50 μA		4.5 V		.001	0.1		0.1	V
	I_{OL} = 8 mA					0.36		0.44	
I_{OZ}	$V_O = V_{CC}$ or GND		5.5 V			± 0.25		± 2.5	μA
I_I	$V_I = V_{CC}$ or GND		5.5 V			± 0.1		± 1	μA
I_{CC}	$V_I = V_{CC}$ or GND,	I_O = 0	5.5 V			4		40	μA
ΔI_{CC}†	One input at 3.4 V,	Other inputs at V_{CC} or GND	5.5 V			1.35		1.5	mA
I_{off}	V_O = 5.5 V		0 V			0.5		5	μA
C_i	$V_I = V_{CC}$ or GND		5 V		2.5	10		10	pF
C_o	$V_O = V_{CC}$ or GND		5 V		3				pF

† This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
t_{PLH}	A	Y	C_L = 15 pF		5.4	7.4	1	8.5	ns
t_{PHL}					5.4	7.4	1	8.5	
t_{PZH}	$\overline{OE}$	Y			7.7	10.4	1	12	ns
t_{PZL}					7.7	10.4	1	12	
t_{PHZ}	$\overline{OE}$	Y			8.3	10.4	1	12	ns
t_{PLZ}					8.3	10.4	1	12	
t_{PLH}	A	Y	C_L = 50 pF		5.9	8.4	1	9.5	ns
t_{PHL}					5.9	8.4	1	9.5	
t_{PZH}	$\overline{OE}$	Y			8.2	11.4	1	13	ns
t_{PZL}					8.2	11.4	1	13	
t_{PHZ}	$\overline{OE}$	Y			8.8	11.4	1	13	ns
t_{PLZ}					8.8	11.4	1	13	

output-skew characteristics, C_L = 50 pF (see Note 4)

PARAMETER		V_{CC}	T_A = 25°C		MIN	MAX	UNIT
			MIN	MAX			
$t_{sk(o)}$	Output skew	5 V ± 0.5 V		1		1	ns

NOTE 4: Characteristics are determined during product characterization and ensured by design.

noise characteristics, V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C (see Note 5)

PARAMETER		MIN	TYP	MAX	UNIT
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.6		V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		–0.6		V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}		4.1		V
$V_{IH(D)}$	High-level dynamic input voltage	2			V
$V_{IL(D)}$	Low-level dynamic input voltage			0.8	V

NOTE 5: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance	C_L = 50 pF,	f = 1 MHz	10	pF

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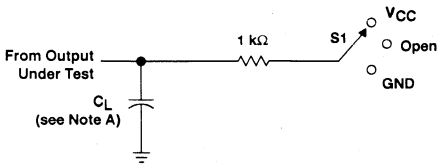
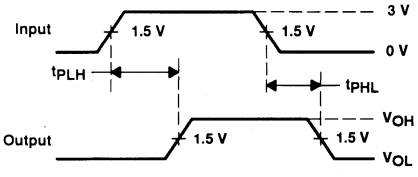
PARAMETER MEASUREMENT INFORMATION

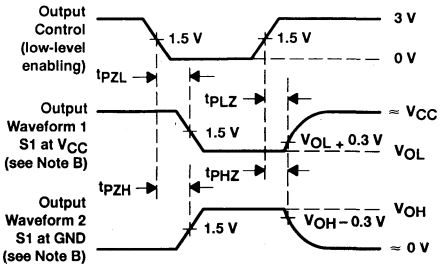


LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND



VOLTAGE WAVEFORMS
DELAY TIMES



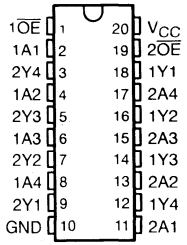
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

- Inputs Are TTL-Voltage Compatible
- *EPIC*™ (Enhanced-Performance Implanted CMOS) Process
- High Latch-Up Immunity Exceeds 300 mA Per JEDEC Standard JESD-17
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW) Packages, and Standard Plastic (N) DIPs

DB, DW, N, OR PW PACKAGE
(TOP VIEW)



description

This octal buffer/driver is designed specifically to improve both the performance and density of 3-state memory-address drivers, clock drivers, and bus-oriented receivers and transmitters.

The SN74AHCT244 is organized as two 4-bit buffers/line drivers with separate output-enable ($\overline{OE}$) inputs. When $\overline{OE}$ is low, the device passes data from the A inputs to the Y outputs. When $\overline{OE}$ is high, the outputs are in the high-impedance state.

The SN74AHCT244 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each buffer)

INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	H
L	L	L
H	X	Z

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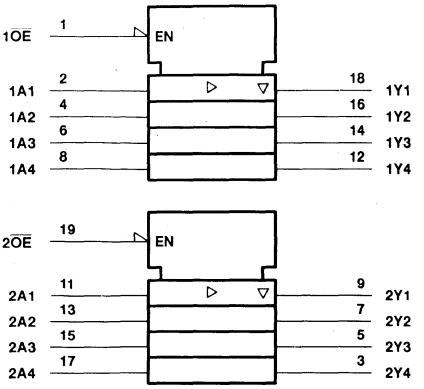
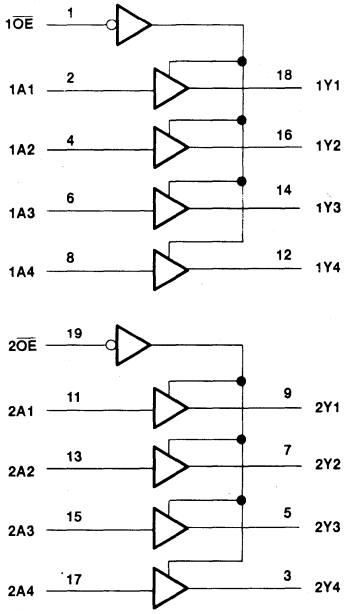
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) ..... − 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... − 20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) ..... ± 25 mA
Continuous current through V_{CC} or GND ..... ± 75 mA
Maximum power dissipation at $T_A = 55°C$ (in still air) (see Note 2): DB package ..... 0.6 W
DW package ..... 1.6 W
N package ..... 1.3 W
PW package ..... 0.7 W
Storage temperature range, T_{stg} ..... −65°C to 150°C

‡Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions(see Note 3)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4.5	5.5	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
V_I	Input voltage	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	V
I_{OH}	High-level output current		−8	mA
I_{OL}	Low-level output current		8	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		20	ns/V
T_A	Operating free-air temperature	−40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
V_{OH}	I_{OH} = − 50 μA	4.5 V	3.15	3.65		3.15		V
	I_{OH} = − 8 mA		2.5			2.4		
V_{OL}	I_{OL} = 50 μA	4.5 V			0.1		0.1	V
	I_{OL} = 8 mA				0.36		0.44	
I_{OZ}	V_O = V_{CC} or GND	5.5 V			±0.25		±2.5	μA
I_I	V_I = V_{CC} or GND	5.5 V			±0.1		±1	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			4		40	μA
ΔI_{CC}†	One input at 3.4 V, Other inputs at V_{CC} or GND	5.5 V			1.35		1.5	mA
I_{off}	V_O = 5.5 V	0 V			0.5		5	μA
C_i	V_I = V_{CC} or GND	5 V		2.5	10		10	pF
C_o	V_O = V_{CC} or GND	5 V		3				pF

† This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

switching characteristics over recommended operating free-air temperature range V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
t_{PLH}	A	Y	C_L = 15 pF		5.4	7.4	1	8.5	ns
t_{PHL}					5.4	7.4	1	8.5	
t_{PZH}	$\overline{OE}$	Y			7.7	10.4	1	12	ns
t_{PZL}					7.7	10.4	1	12	
t_{PHZ}	$\overline{OE}$	Y			5	9.4	1	10	ns
t_{PLZ}					5	9.4	1	10	
t_{PLH}	A	Y	C_L = 50 pF		5.9	8.4	1	9.5	ns
t_{PHL}					5.9	8.4	1	9.5	
t_{PZH}	$\overline{OE}$	Y			8.2	11.4	1	13	ns
t_{PZL}					8.2	11.4	1	13	
t_{PHZ}	$\overline{OE}$	Y			8.8	11.4	1	13	ns
t_{PLZ}					8.8	11.4	1	13	

output-skew characteristics, C_L = 50 pF (see Note 4)

PARAMETER		V_{CC}	T_A = 25°C		MIN	MAX	UNIT
			MIN	MAX			
$t_{sk(o)}$	Output skew	5 V ± 0.5 V		1		1	ns

NOTE 4: Characteristics are determined during product characterization and ensured by design.

noise characteristics, V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C (see Note 5)

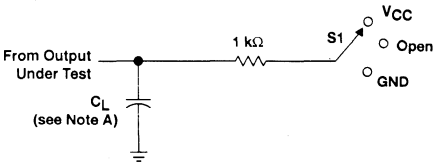
PARAMETER		MIN	TYP	MAX	UNIT
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.7		V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		–0.7		V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}		4.1		V
$V_{IH(D)}$	High-level dynamic input voltage	2			V
$V_{IL(D)}$	Low-level dynamic input voltage			0.8	V

NOTE 5: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

operating characteristics, V_{CC} = 5 V, T_A = 25°C

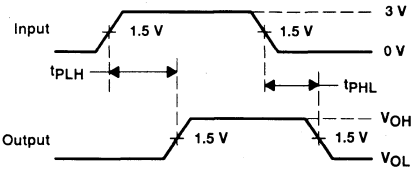
PARAMETER		TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance	C_L = 50 pF,	f = 1 MHz	8.2	pF

PARAMETER MEASUREMENT INFORMATION

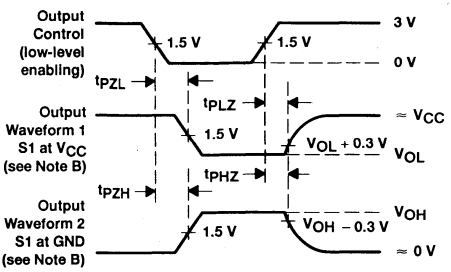


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND

LOAD CIRCUIT



VOLTAGE WAVEFORMS
DELAY TIMES



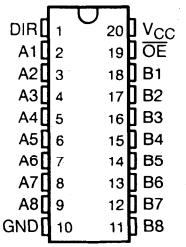
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

- Inputs Are TTL-Voltage Compatible
- *EPIC*™ (Enhanced-Performance Implanted CMOS) Process
- High Latch-Up Immunity Exceeds 300 mA Per JEDEC Standard JESD-17
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW) Packages, and Standard Plastic (N) DIPs

DB, DW, N, OR PW PACKAGE
(TOP VIEW)



description

This octal bus transceiver is designed for asynchronous two-way communication between data buses. The control-function implementation minimizes external timing requirements.

The SN74AHCT245 allows data transmission from the A bus to the B bus or from the B bus to the A bus, depending upon the logic level at the direction-control (DIR) input. The output-enable ($\overline{OE}$) input can be used to disable the device so that the buses are effectively isolated.

The SN74AHCT245 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE

INPUTS		OUTPUT
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

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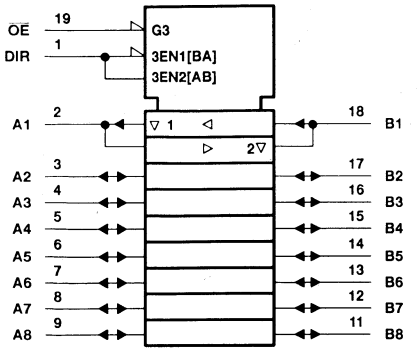
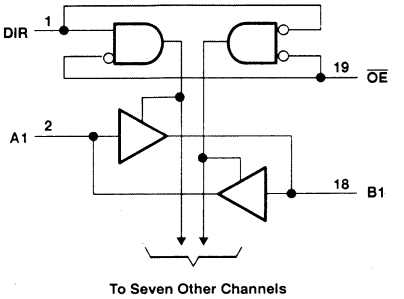
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... –0.5 V to 7 V
Output voltage range, V_O (see Note 1) ..... –0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) ..... –20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... –20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) ..... ±25 mA
Continuous current through V_{CC} or GND ..... ±75 mA
Maximum power dissipation at $T_A = 55°C$ (in still air) (see Note 2): DB package ..... 0.6 W
DW package ..... 1.6 W
N package ..... 1.3 W
PW package ..... 0.7 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4.5	5.5	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
V_I	Input voltage	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	V
I_{OH}	High-level output current		–8	mA
I_{OL}	Low-level output current		8	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		20	ns/V
T_A	Operating free-air temperature	–40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC}	T_A = 25°C			MIN	MAX	UNIT
					MIN	TYP	MAX			
V_{OH}		I_{OH} = –50 μA		4.5 V	3.15	3.65		3.15		V
		I_{OH} = –8 mA			2.5			2.4		
V_{OL}		I_{OL} = 50 μA		4.5 V			0.1		0.1	V
		I_{OL} = 8 mA					0.36		0.44	
I_{OZ}	A or B inputs†	$V_O = V_{CC}$ or GND		5.5 V			±0.25		±2.5	μA
I_I	$\overline{OE}$ or DIR	$V_I = V_{CC}$ or GND		5.5 V			±0.1		±1	μA
I_{CC}		$V_I = V_{CC}$ or GND,	I_O = 0	5.5 V			4		40	μA
ΔI_{CC}‡		One input at 3.4 V,	Other inputs at V_{CC} or GND	5.5 V			1.35		1.5	mA
I_{off}		V_O = 5.5 V		0 V			0.5		5	μA
C_i	$\overline{OE}$ or DIR	$V_I = V_{CC}$ or GND		5 V		2.5	10		10	pF
C_{io}	A or B inputs	$V_I = V_{CC}$ or GND		5 V		4				pF

† For I/O ports, the parameter I_{OZ} includes the input leakage current.
‡ This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
t_{PLH}	A or B	B or A	C_L = 15 pF		4.5	7.7	1	8.5	ns
t_{PHL}					4.5	7.7	1	8.5	
t_{PZH}	$\overline{OE}$	A or B	C_L = 15 pF		8.9	13.8	1	15	ns
t_{PZL}					8.9	13.8	1	15	
t_{PHZ}	$\overline{OE}$	A or B	C_L = 15 pF		9.2	14.4	1	15.5	ns
t_{PLZ}					9.2	14.4	1	15.5	
t_{PLH}	A or B	B or A	C_L = 50 pF		5.3	8.7	1	9.5	ns
t_{PHL}					5.3	8.7	1	9.5	
t_{PZH}	$\overline{OE}$	A or B	C_L = 50 pF		9.7	14.8	1	16	ns
t_{PZL}					9.7	14.8	1	16	
t_{PHZ}	$\overline{OE}$	A or B	C_L = 50 pF		10	15.4	1	16.5	ns
t_{PLZ}					10	15.4	1	16.5	

output-skew characteristics, C_L = 50 pF (see Note 4)

PARAMETER		V_{CC}	T_A = 25°C		MIN	MAX	UNIT
			MIN	MAX			
$t_{sk(o)}$	Output skew	5 V ± 0.5 V		1		1	ns

NOTE 4: Characteristics are determined during product characterization and ensured by design.

noise characteristics, V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C (see Note 5)

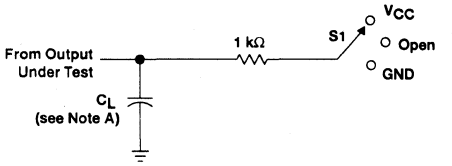
PARAMETER		MIN	TYP	MAX	UNIT
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}		4		V
$V_{IH(D)}$	High-level dynamic input voltage	2			V
$V_{IL(D)}$	Low-level dynamic input voltage			0.8	V

NOTE 5: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

operating characteristics, V_{CC} = 5 V, T_A = 25°C

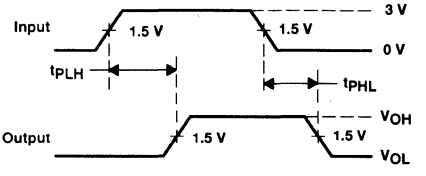
PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per transceiver	C_L = 50 pF, f = 1 MHz	13	pF

PARAMETER MEASUREMENT INFORMATION

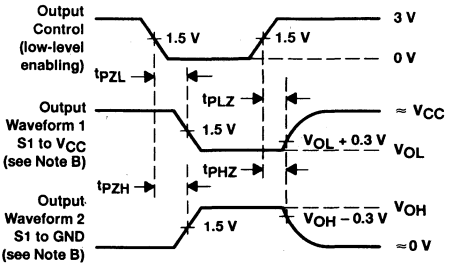


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND

LOAD CIRCUIT



VOLTAGE WAVEFORMS
DELAY TIMES



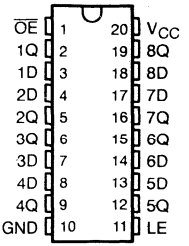
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

- **Inputs Are TTL-Voltage Compatible**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW) Packages, and Standard Plastic (N) DIPs**

DB, DW, N, OR PW PACKAGE
(TOP VIEW)



description

The SN74AHCT373 is an octal-transparent D-type latch. When the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is low, the Q outputs are latched at the logic levels of the D inputs.

A buffered output-enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.

$\overline{OE}$ does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN74AHCT373 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each latch)

INPUTS			OUTPUT
$\overline{OE}$	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

PRODUCT PREVIEW

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PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.

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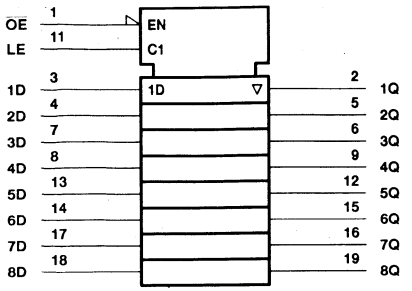
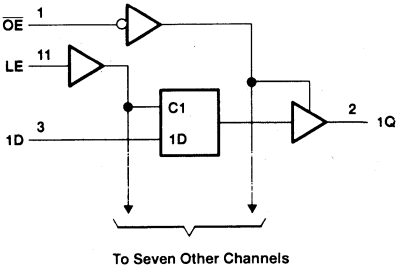
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... –0.5 V to 7 V
Output voltage range, V_O (see Note 1) ..... –0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) ..... – 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... – 20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ± 25 mA
Continuous current through V_{CC} or GND ..... ± 75 mA
Maximum power dissipation at T_A = 55°C (in still air)(see Note 2): DB package ..... 0.6 W
DW package ..... 1.6 W
N package ..... 1.3 W
PW package ..... 0.7 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

‡Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4.5	5.5	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
V_I	Input voltage	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	V
I_{OH}	High-level output current		–8	mA
I_{OL}	Low-level output current		8	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		20	ns/V
T_A	Operating free-air temperature	– 40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
V_{OH}	I_{OH} = – 50 μA		4.5 V	3.15	3.65		3.15		V
	I_{OH} = – 8 mA			2.5			2.4		
V_{OL}	I_{OL} = 50 μA		4.5 V			0.1		0.1	V
	I_{OL} = 8 mA					0.36		0.44	
I_{OZ}	V_O = V_{CC} or GND		5.5 V			± 0.25		± 2.5	μA
I_I	V_I = V_{CC} or GND		5.5 V			± 0.1		± 1	μA
I_{CC}	V_I = V_{CC} or GND,	I_O = 0	5.5 V			4		40	μA
ΔI_{CC}†	One input at 3.4 V,	Other inputs at V_{CC} or GND	5.5 V			1.35		1.5	mA
I_{off}	V_O = 5.5 V		0 V			0.5		5	μA
C_i	V_I = V_{CC} or GND		5 V		4				pF
C_o	V_O = V_{CC} or GND		5 V		6				pF

† This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

		T_A = 25°C		MIN	MAX	UNIT
		MIN	MAX			
t_w	Pulse duration, $\overline{LE}$ high	5		5		ns
t_{su}	Setup time, data before $\overline{LE}$↓	4		4		ns
t_h	Hold time, data after $\overline{LE}$↓	1		1		ns

switching characteristics over recommended free-air temperature operating range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C		MIN	MAX	UNIT
				MIN	MAX			
t_{PLH}	D	Q	C_L = 15 pF		7.2	1	8.5	ns
t_{PHL}					7.2	1	8.5	
t_{PLH}	LE	Q			7.2	1	8.5	ns
t_{PHL}					7.2	1	8.5	
t_{PZH}	$\overline{OE}$	Q			8.1	1	9.5	ns
t_{PZL}					8.1	1	9.5	
t_{PHZ}	$\overline{OE}$	Q						ns
t_{PLZ}								
t_{PLH}	D	Q	C_L = 50 pF		9.2	1	10.5	ns
t_{PHL}					9.2	1	10.5	
t_{PLH}	LE	Q			9.2	1	10.5	ns
t_{PHL}					9.2	1	10.5	
t_{PZH}	$\overline{OE}$	Q			10.1	1	11.5	ns
t_{PZL}					10.1	1	11.5	
t_{PHZ}	$\overline{OE}$	Q			9.2	1	10.5	ns
t_{PLZ}					9.2	1	10.5	

PRODUCT PREVIEW

noise characteristics, V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C (see Note 4)

PARAMETER		MIN	TYP	MAX	UNIT
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}			0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}			−0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}				V
$V_{IH(D)}$	High-level dynamic input voltage	2			V
$V_{IL(D)}$	Low-level dynamic input voltage			0.8	V

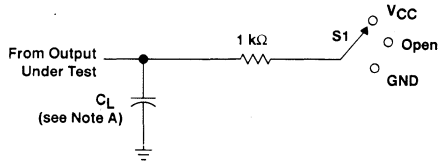
NOTE 4: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_{pd}	Power dissipation capacitance	C_L = 50 pF, f = 1 MHz		27		pF

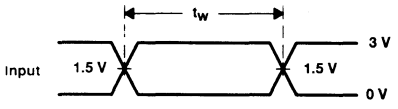
PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

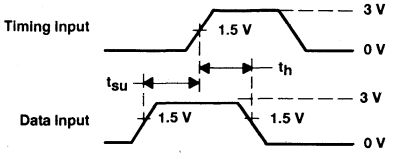


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND

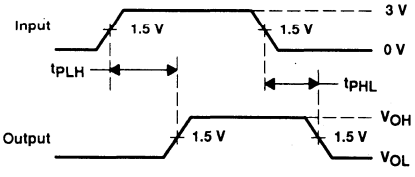
LOAD CIRCUIT



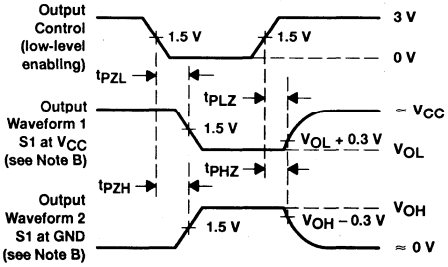
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

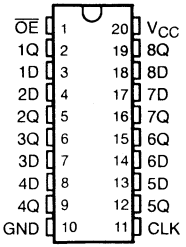
NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PRODUCT PREVIEW

- **Inputs Are TTL-Voltage Compatible**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW) Packages, and Standard Plastic (N) DIPs**

DB, DW, N, OR PW PACKAGE
(TOP VIEW)



description

The SN74AHCT374 is an octal edge-triggered D-type flip-flop that features 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. This device is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

On the positive transition of the clock (CLK) input, the Q outputs are set to the logic levels of the data (D) inputs.

A buffered output-enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without interface or pullup components.

$\overline{OE}$ does not affect internal operations of the flip-flop. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN74AHCT374 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each flip-flop)

INPUTS			OUTPUT
$\overline{OE}$	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	H or L	X	Q_0
H	X	X	Z

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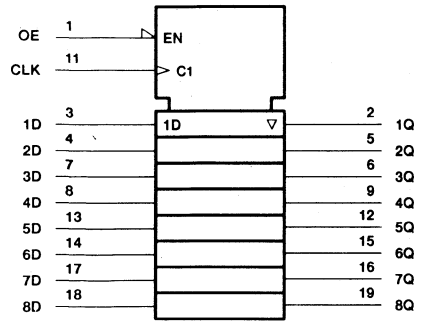
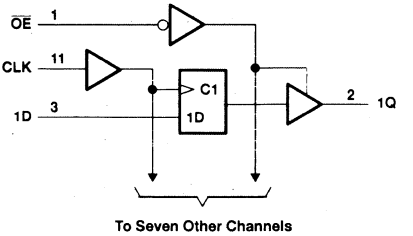
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



PRODUCT PREVIEW

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) ..... ± 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ± 20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) ..... ± 25 mA
Continuous current through V_{CC} or GND ..... ± 75 mA
Maximum power dissipation at $T_A = 55°C$ (in still air) (see Note 2): DB package ..... 0.6 W
DW package ..... 1.6 W
N package ..... 1.3 W
PW package ..... 0.7 W
Storage temperature range, T_{stg} ..... −65°C to 150°C

‡Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4.5	5.5	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
V_I	Input voltage	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	V
I_{OH}	High-level output current		–8	mA
I_{OL}	Low-level output current		8	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		20	ns/V
T_A	Operating free-air temperature	– 40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
V_{OH}	I_{OH} = – 50 μA		4.5 V	3.15	3.65		3.15		V
	I_{OH} = – 8 mA			2.5			2.4		
V_{OL}	I_{OL} = 50 μA		4.5 V			0.1		0.1	V
	I_{OL} = 8 mA					0.36		0.44	
I_{OZ}	$V_O = V_{CC}$ or GND,	$V_I = V_{IH}$ or V_{IL}	5.5 V			± 0.25		± 2.5	μA
I_I	$V_I = V_{CC}$ or GND		5.5 V			± 0.1		± 1	μA
I_{CC}	$V_I = V_{CC}$ or GND,	I_O = 0	5.5 V			4		40	μA
ΔI_{CC}†	One input at 3.4 V,	Other inputs at V_{CC} or GND	5.5 V			1.35		1.5	mA
I_{off}	V_O = 5.5 V		0 V			0.5		5	μA
C_i	$V_I = V_{CC}$ or GND		5 V		4				pF
C_o	$V_I = V_{CC}$ or GND		5 V		6				pF

† This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted)(see Figure 1)

		T_A = 25°C		MIN	MAX	UNIT
		MIN	MAX			
t_w	Pulse duration, CLK high or low	5		5		ns
t_{su}	Setup time, data before CLK↑	5		5.5		ns
t_h	Hold time, data after CLK↑	1.5		1.5		ns

PRODUCT PREVIEW

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted)(see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
f_{max}			C_L = 15 pF	130			110		MHz
			C_L = 50 pF	85			75		
t_{PLH}	CLK	Q	C_L = 15 pF			8.1	1	9.5	ns
t_{PHL}						8.1	1	9.5	
t_{PZH}	$\overline{OE}$	Q				7.6	1	9	ns
t_{PZL}						7.6	1	9	
t_{PHZ}	OE	Q							ns
t_{PLZ}									
t_{PLH}	CLK	Q	C_L = 50 pF			10.1	1	11.5	ns
t_{PHL}						10.1	1	11.5	
t_{PZH}	$\overline{OE}$	Q				9.6	1	11	ns
t_{PZL}						9.6	1	11	
t_{PHZ}	$\overline{OE}$	Q				8.8	1	10	ns
t_{PLZ}						8.8	1	10	

noise characteristics, V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C (see Note 4)

PARAMETER		MIN	TYP	MAX	UNIT
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}			0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}			−0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}				V
$V_{IH(D)}$	High-level dynamic input voltage	2			V
$V_{IL(D)}$	Low-level dynamic input voltage			0.8	V

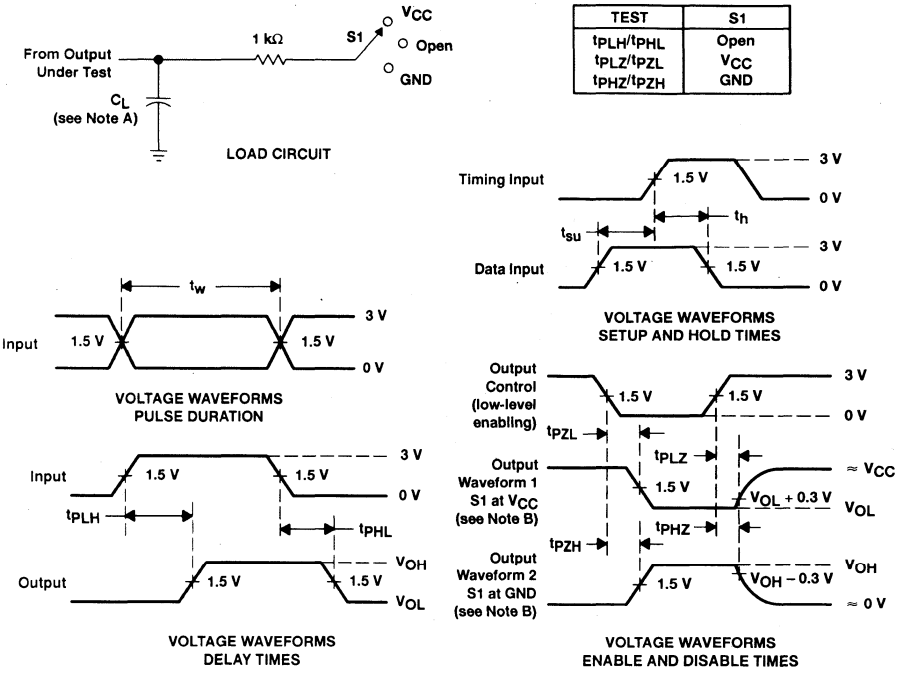
NOTE 4: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_{pd}	Power dissipation capacitance	C_L = 50 pF, f = 1 MHz		40		pF

PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION



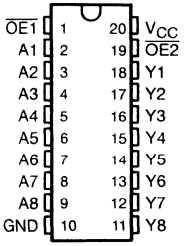
NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PRODUCT PREVIEW

- **Inputs Are TTL-Voltage Compatible**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW) Packages, and Standard Plastic (N) DIPs**

DB, DW, N, OR PW PACKAGE
(TOP VIEW)



description

The SN74AHCT540 octal buffer/driver is ideal for driving bus lines or buffer memory address registers. This device features inputs and outputs on opposite sides of the package to facilitate printed-circuit-board layout.

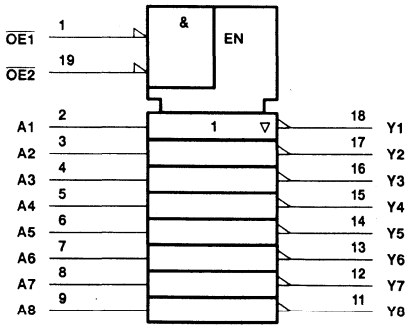
The 3-state control gate is a 2-input AND gate with active-low inputs so that if either output-enable ($\overline{OE1}$ or $\overline{OE2}$) input is high, all corresponding outputs are in the high-impedance state. The outputs provide inverted data when they are not in the high-impedance state.

The SN74AHCT540 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE

INPUTS			OUTPUT
$\overline{OE1}$	$\overline{OE2}$	A	Y
L	L	L	H
L	L	H	L
H	X	X	Z
X	H	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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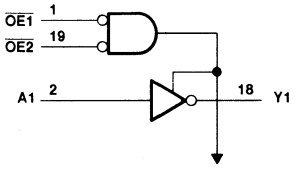
logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... –0.5 V to 7 V
Output voltage range, V_O (see Note 1) ..... –0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) ..... –20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... –20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) ..... ±25 mA
Continuous current through V_{CC} or GND ..... ±75 mA
Maximum power dissipation at $T_A = 55°C$ (in still air) (see Note 2): DB package ..... 0.6 W
DW package ..... 1.6 W
N package ..... 1.3 W
PW package ..... 0.7 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4.5	5.5	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
V_I	Input voltage	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	V
I_{OH}	High-level output current		–8	mA
I_{OL}	Low-level output current		8	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		20	ns/V
T_A	Operating free-air temperature	–40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
V_{OH}	I_{OH} = –50 μA	4.5 V	3.15	3.65		3.15		V
	I_{OH} = –8 mA		2.5			2.4		
V_{OL}	I_{OL} = 50 μA	4.5 V			0.1		0.1	V
	I_{OL} = 8 mA				0.36		0.44	
I_{OZ}	V_O = V_{CC} or GND	5.5 V			±0.25		±2.5	μA
I_I	V_I = V_{CC} or GND	5.5 V			±0.1		±1	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			4		40	μA
ΔI_{CC}†	One input at 3.4 V, Other inputs at GND or V_{CC}	5.5 V			1.35		1.5	mA
I_{off}	V_O = 5.5 V	0 V			0.5		5	μA
C_i	V_I = V_{CC} or GND	5 V		4	10		10	pF
C_o	V_O = V_{CC} or GND	5 V		9				pF

† This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
t_{PLH}	A	Y	C_L = 15 pF						ns
t_{PHL}									
t_{PZH}	$\overline{OE}$	Y	C_L = 15 pF						ns
t_{PZL}									
t_{PHZ}	$\overline{OE}$	Y	C_L = 15 pF						ns
t_{PLZ}									
t_{PLH}	A	Y	C_L = 50 pF						ns
t_{PHL}									
t_{PZH}	$\overline{OE}$	Y	C_L = 50 pF						ns
t_{PZL}									
t_{PHZ}	$\overline{OE}$	Y	C_L = 50 pF						ns
t_{PLZ}									

output-skew characteristics, C_L = 50 pF (see Note 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
$t_{sk(o)}$	A	Y	5 V ± 0.5 V			1		1	ns

NOTE 4: Characteristics are determined during product characterization and ensured by design.

PRODUCT PREVIEW

noise characteristics, V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C (see Note 5)

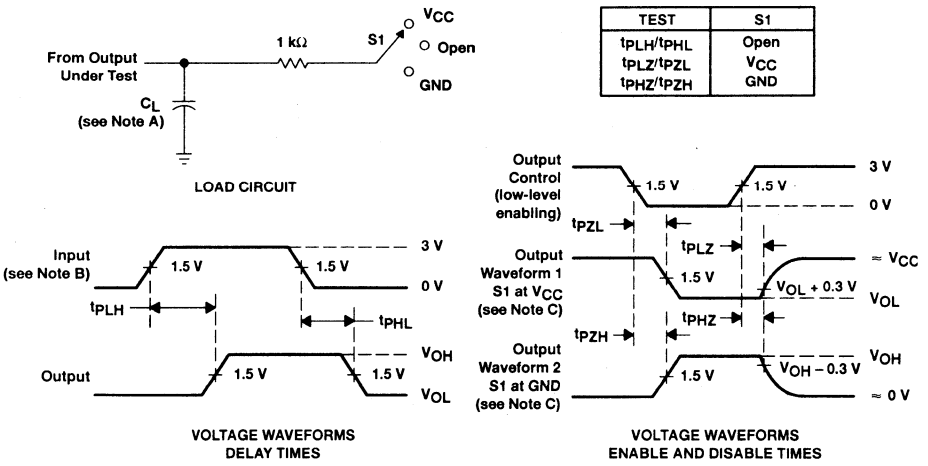
PARAMETER		MIN	TYP	MAX	UNIT
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}			0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}			−0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}				V
$V_{IH(D)}$	High-level dynamic input voltage	2			V
$V_{IL(D)}$	Low-level dynamic input voltage			0.8	V

NOTE 5: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	C_L = 50 pF, f = 1 MHz		pF

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PRODUCT PREVIEW

TEXAS INSTRUMENTS
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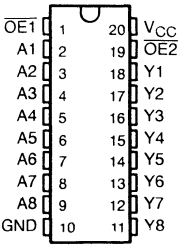
- Inputs Are TTL-Voltage Compatible
- *EPIC*™ (Enhanced-Performance Implanted CMOS) Process
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW) Packages, and Standard Plastic (N) DIPs

DB, DW, N, OR PW PACKAGE
(TOP VIEW)



description

The SN74AHCT541 octal buffer/driver is ideal for driving bus lines or buffer memory address registers. This device features inputs and outputs on opposite sides of the package to facilitate printed-circuit-board layout.

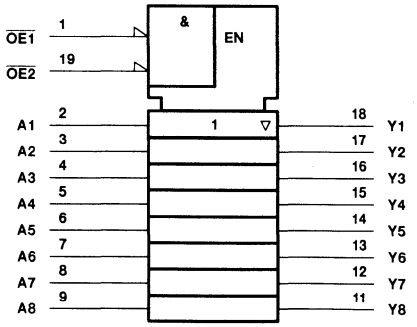
The 3-state control gate is a 2-input AND gate with active-low inputs so that if either output-enable ($\overline{OE1}$ or $\overline{OE2}$) input is high, all corresponding outputs are in the high-impedance state. The outputs provide noninverted data when they are not in the high-impedance state.

The SN74AHCT541 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE

INPUTS			OUTPUT
$\overline{OE1}$	$\overline{OE2}$	A	Y
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

PRODUCT PREVIEW

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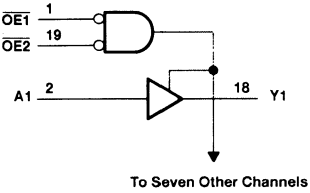
logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... –0.5 V to 7 V
Output voltage range, V_O (see Note 1) ..... –0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) ..... –20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... –20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) ..... ±25 mA
Continuous current through V_{CC} or GND ..... ±75 mA
Maximum power dissipation at $T_A = 55°C$ (in still air)(see Note 2): DB package ..... 0.6 W
DW package ..... 1.6 W
N package ..... 1.3 W
PW package ..... 0.7 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4.5	5.5	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
V_I	Input voltage	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	V
I_{OH}	High-level output current		–8	mA
I_{OL}	Low-level output current		8	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		20	ns/V
T_A	Operating free-air temperature	–40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
V_{OH}	I_{OH} = –50 µA		4.5 V	3.15	3.65		3.15		V
	I_{OH} = –8 mA			2.5			2.4		
V_{OL}	I_{OL} = 50 µA		4.5 V			0.1		0.1	V
	I_{OL} = 8 mA					0.36		0.44	
I_{OZ}	V_O = V_{CC} or GND		5.5 V			±0.25		±2.5	µA
I_I	V_I = V_{CC} or GND		5.5 V			±0.1		±1	µA
I_{CC}	V_I = V_{CC} or GND,	I_O = 0	5.5 V			4		40	µA
ΔI_{CC}†	One input at 3.4 V,	Other inputs at GND or V_{CC}	5.5 V			1.35		1.5	mA
I_{off}	V_O = 5.5 V		0 V			0.5		5	µA
C_i	V_I = V_{CC} or GND		5 V		4	10		10	pF
C_o	V_O = V_{CC} or GND		5 V		9				pF

† This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
t_{PLH}	A	Y	C_L = 15 pF						ns
t_{PHL}									
t_{PZH}	$\overline{OE}$	Y	C_L = 15 pF						ns
t_{PZL}									
t_{PHZ}	$\overline{OE}$	Y	C_L = 15 pF						ns
t_{PLZ}									
t_{PLH}	A	Y	C_L = 50 pF						ns
t_{PHL}									
t_{PZH}	$\overline{OE}$	Y	C_L = 50 pF						ns
t_{PZL}									
t_{PHZ}	$\overline{OE}$	Y	C_L = 50 pF						ns
t_{PLZ}									

output-skew characteristics, C_L = 50 pF (see Note 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
$t_{sk(o)}$	A	Y	5 V ± 0.5 V			1		1	ns

NOTE 4: Characteristics are determined during product characterization and ensured by design.

PRODUCT PREVIEW

noise characteristics, V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C (see Note 5)

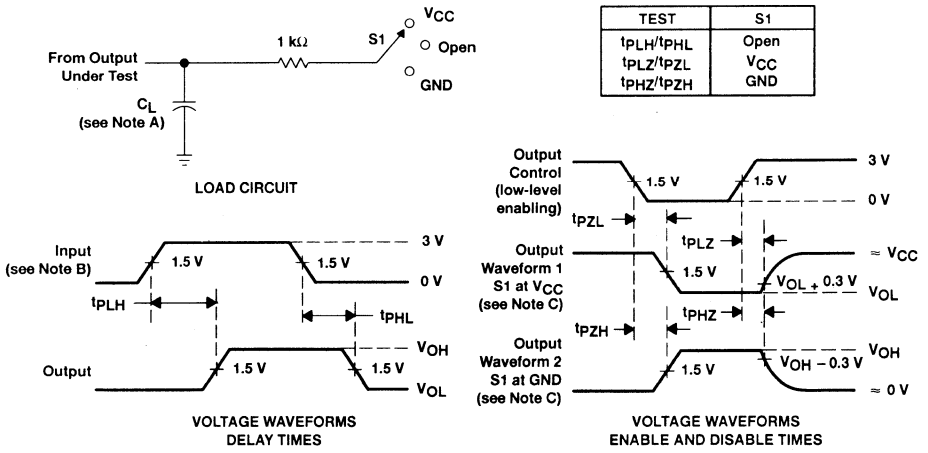
PARAMETER		MIN	TYP	MAX	UNIT
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}			0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}			–0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}				V
$V_{IH(D)}$	High-level dynamic input voltage	2			V
$V_{IL(D)}$	Low-level dynamic input voltage			0.8	V

NOTE 5: Characteristics are determined during product characterization and ensured by design for surface-mount packages only

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	C_L = 50 pF, f = 1 MHz		pF

PARAMETER MEASUREMENT INFORMATION



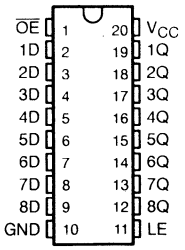
NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PRODUCT PREVIEW

- **Inputs Are TTL-Voltage Compatible**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW) Packages, and Standard Plastic (N) DIPs**

DB, DW, N, OR PW PACKAGE
(TOP VIEW)



description

The SN74AHCT573 is an octal-transparent D-type latch. When the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is low, the Q outputs are latched at the logic levels of the D inputs.

A buffered output-enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.

$\overline{OE}$ does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN74AHCT573 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE
(each latch)

INPUTS			OUTPUT
$\overline{OE}$	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

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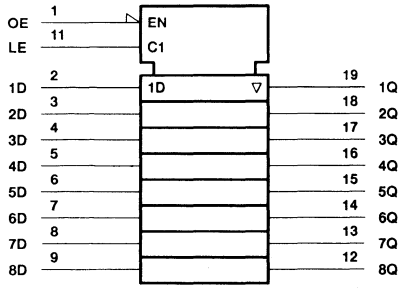
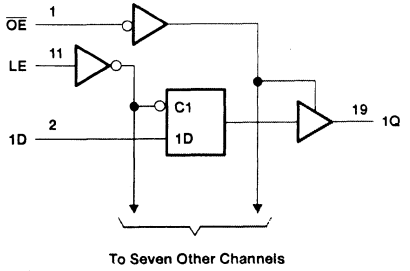
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) ..... − 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... − 20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ± 25 mA
Continuous current through V_{CC} or GND ..... ± 75 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2): DB package ..... 0.6 W
DW package ..... 1.6 W
N package ..... 1.3 W
PW package ..... 0.7 W
Storage temperature range, T_{stg} ..... −65°C to 150°C

‡Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4.5	5.5	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
V_I	Input voltage	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	V
I_{OH}	High-level output current		−8	mA
I_{OL}	Low-level output current		8	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		20	ns/V
T_A	Operating free-air temperature	−40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
V_{OH}	I_{OH} = – 50 μA		4.5 V	3.15	3.65		3.15		V
	I_{OH} = –8 mA			2.5			2.4		
V_{OL}	I_{OL} = 50 μA		4.5 V			0.1		0.1	V
	I_{OL} = 8 mA					0.36		0.44	
I_{OZ}	V_O = V_{CC} or GND		5.5 V			± 0.25		± 2.5	μA
I_I	V_I = V_{CC} or GND		5.5 V			± 0.1		± 1	μA
I_{CC}	V_I = V_{CC} or GND,	I_O = 0	5.5 V			4		40	μA
ΔI_{CC}†	One input at 3.4 V,	Other inputs at V_{CC} or GND	5.5 V			1.35		1.5	mA
I_{off}	V_O = 5.5 V		0 V			0.5		5	μA
C_i	V_I = V_{CC} or GND		5 V		4	10		10	pF
C_o	V_O = V_{CC} or GND		5 V		6				pF

† This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

		T_A = 25°C		MIN	MAX	UNIT
		MIN	MAX			
t_w	Pulse duration, $\overline{LE}$ high	5		5		ns
t_{su}	Setup time, data before $\overline{LE}$↓	3.5		3.5		ns
t_h	Hold time, data after $\overline{LE}$↓	1.5		1.5		ns

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C		MIN	MAX	UNIT
				MIN	MAX			
t_{PLH}	D	Q	C_L = 15 pF		6.8	1	8	ns
t_{PHL}					6.8	1	8	
t_{PLH}	LE	Q			7.7	1	9	ns
t_{PHL}					7.7	1	9	
t_{PZH}	$\overline{OE}$	Q			7.7	1	9	ns
t_{PZL}					7.7	1	9	
t_{PHZ}	$\overline{OE}$	Q						ns
t_{PLZ}								
t_{PLH}	D	Q	C_L = 50 pF		8.8	1	10	ns
t_{PHL}					8.8	1	10	
t_{PLH}	LE	Q			9.7	1	11	ns
t_{PHL}					9.7	1	11	
t_{PZH}	$\overline{OE}$	Q			9.7	1	11	ns
t_{PZL}					9.7	1	11	
t_{PHZ}	$\overline{OE}$	Q			9.7	1	11	ns
t_{PLZ}					9.7	1	11	

PRODUCT PREVIEW

output-skew characteristics, C_L = 50 pF (see Note 4)

PARAMETER		V_{CC}	T_A = 25°C		MIN	MAX	UNIT
			MIN	MAX			
$t_{sk(o)}$	Output skew	5 V ± 0.5 V		1		1	ns

NOTE 4: Characteristics are determined during product characterization and ensured by design.

noise characteristics, V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C (see Note 5)

PARAMETER		MIN	TYP	MAX	UNIT
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}			0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}			−0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}				V
$V_{IH(D)}$	High-level dynamic input voltage	2			V
$V_{IL(D)}$	Low-level dynamic input voltage			0.8	V

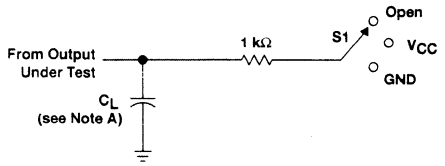
NOTE 5: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	C_L = 50 pF, f = 1 MHz	25	pF

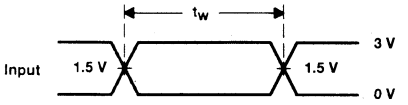
PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

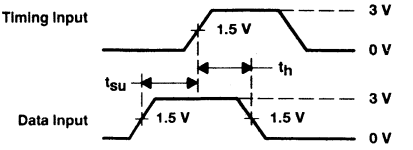


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND

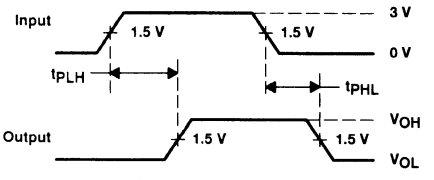
LOAD CIRCUIT



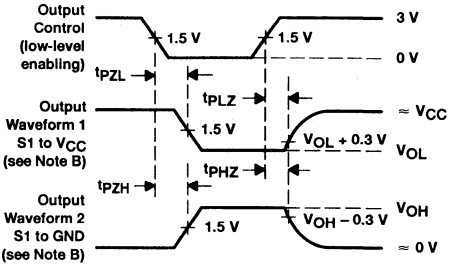
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

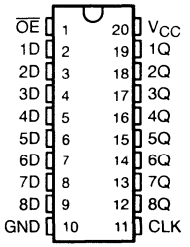
NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PRODUCT PREVIEW

- **Inputs Are TTL-Voltage Compatible**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW) Packages, and Standard Plastic (N) DIPs**

DB, DW, N, OR PW PACKAGE
(TOP VIEW)



description

The SN74AHCT574 is an octal edge-triggered D-type flip-flop that features 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. This device is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

On the positive transition of the clock (CLK) input, the Q outputs are set to the logic levels of the data (D) inputs.

A buffered output-enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without interface or pullup components.

$\overline{OE}$ does not affect internal operations of the flip-flop. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN74AHCT574 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each flip-flop)

INPUTS			OUTPUT
$\overline{OE}$	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	L or H	X	Q_0
H	X	X	Z

PRODUCT PREVIEW

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PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.

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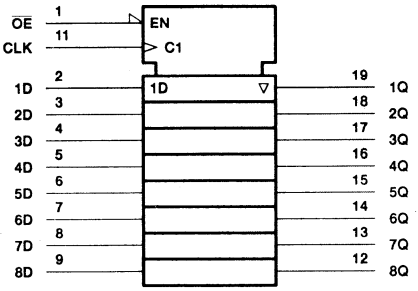
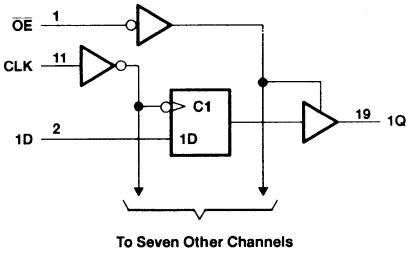
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



PRODUCT PREVIEW

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... –0.5 V to 7 V
Output voltage range, V_O (see Note 1) ..... –0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) ..... –20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... –20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±25 mA
Continuous current through V_{CC} or GND ..... ±75 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2): DB package ..... 0.6 W
DW package ..... 1.6 W
N package ..... 1.3 W
PW package ..... 0.7 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

‡Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4.5	5.5	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
V_I	Input voltage	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	V
I_{OH}	High-level output current		–8	mA
I_{OL}	Low-level output current		8	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		20	ns/V
T_A	Operating free-air temperature	–40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
V_{OH}	I_{OH} = –50 μA	4.5 V	3.15	3.65		3.15		V
	I_{OH} = –8 mA		2.5			2.4		
V_{OL}	I_{OL} = 50 μA	4.5 V			0.1		0.1	V
	I_{OL} = 8 mA				0.36		0.44	
I_{OZ}	$V_O = V_{CC}$ or GND	5.5 V			±0.25		±2.5	μA
I_I	$V_I = V_{CC}$ or GND	5.5 V			±0.1		±1	μA
I_{CC}	$V_I = V_{CC}$ or GND, I_O = 0	5.5 V			4		40	μA
ΔI_{CC}†	One input at 3.4 V, Other inputs at V_{CC} or GND	5.5 V			1.35		1.5	mA
I_{off}	V_O = 5.5 V	0 V			0.5		5	μA
C_i	$V_I = V_{CC}$ or GND	5 V		4.5				pF
C_o	$V_O = V_{CC}$ or GND	5 V		15				pF

† This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

		T_A = 25°C		MIN	MAX	UNIT
		MIN	MAX			
t_w	Pulse duration, CLK high or low	5		5.5		ns
t_{su}	Setup time, data before CLK↑	3.5		3.5		ns
t_h	Hold time, data after CLK↑	1.5		1.5		ns

PRODUCT PREVIEW

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
f_{max}			C_L = 15 pF	130	180		110		MHz
			C_L = 50 pF	85	115		75		
t_{PLH}	CLK	Q	C_L = 15 pF			8.6	1	10	ns
t_{PHL}						8.6	1	10	
t_{PZH}	$\overline{OE}$	Q	C_L = 15 pF			9	1	10.5	ns
t_{PZL}						9	1	10.5	
t_{PHZ}	$\overline{OE}$	Q	C_L = 15 pF						ns
t_{PLZ}									
t_{PLH}	CLK	Q	C_L = 50 pF			10.6	1	12	ns
t_{PHL}						10.6	1	12	
t_{PZH}	$\overline{OE}$	Q	C_L = 50 pF			11	1	12.5	ns
t_{PZL}						11	1	12.5	
t_{PHZ}	$\overline{OE}$	Q	C_L = 50 pF			10.1	1	11.5	ns
t_{PLZ}						10.1	1	11.5	

output-skew characteristics over recommended operating free-air temperature range, C_L = 50 pF (see Note 4)

PARAMETER		V_{CC}	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
$t_{sk(o)}$	Output skew	5 V ± 0.5 V			1		1	ns

NOTE 4: Characteristics are determined during product characterization and ensured by design.

noise characteristics, V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C (see Note 5)

PARAMETER		MIN	TYP	MAX	UNIT
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}			0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}			–0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}				V
$V_{IH(D)}$	High-level dynamic input voltage	2			V
$V_{IL(D)}$	Low-level dynamic input voltage			0.8	V

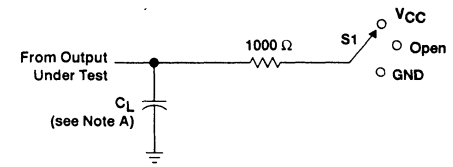
NOTE 5: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	C_L = 50 pF, f = 1 MHz	40	pF

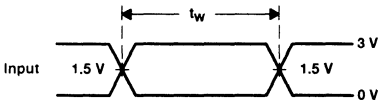
PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

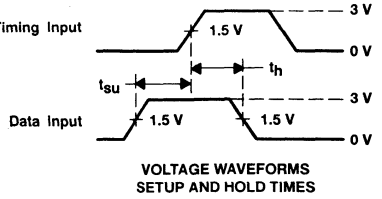


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND

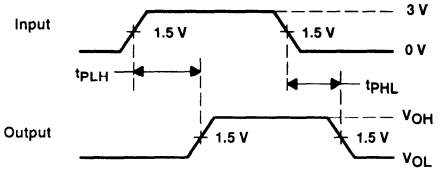
LOAD CIRCUIT



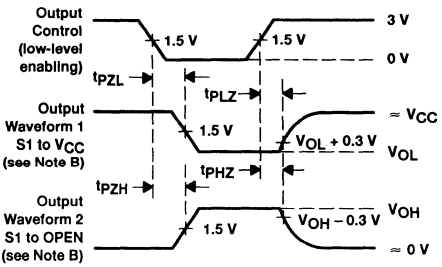
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PRODUCT PREVIEW

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AHCT Data Sheets 3
Mechanical Data 4
AHC04 Qualification Data A
AHCT04 Qualification Data B
AHC245 Qualification Data C
AHCT245 Qualification Data D

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DB (R-PDSO-G**) 4–6
DW (R-PDSO-G**) 4–7
N (R-PDIP-T**) 4–8
PW (R-PDSO-G**) 4–9

Electrical characteristics presented in this data book, unless otherwise noted, apply for the circuit type(s) listed in the page heading regardless of package. The availability of a circuit function in a particular package is denoted by an alphabetical reference above the pin-connection diagram(s). These alphabetical references refer to mechanical outline drawings shown in this section.

Factory orders for circuits described in this catalog should include a four-part type number as explained in the following example.

EXAMPLE: SN 74AHC244 DB LE

Prefix

SN = Standard prefix
SNJ = MIL-STD-883 processed and screened per JEDEC Standard 101

Unique Circuit Description

MUST CONTAIN SEVEN TO ELEVEN CHARACTERS

Examples: 74AHC00
74AHCT245

Package

MUST CONTAIN ONE TO THREE LETTERS

D, DW = plastic small-outline package
DB = plastic shrink small-outline package
N = plastic dual-in-line package
PW = plastic thin shrink small-outline package
(from pin-connection diagram on individual data sheet)

Tape and Reel Packaging

Valid for surface-mount packages only. All orders for tape and reel must be for whole reels.

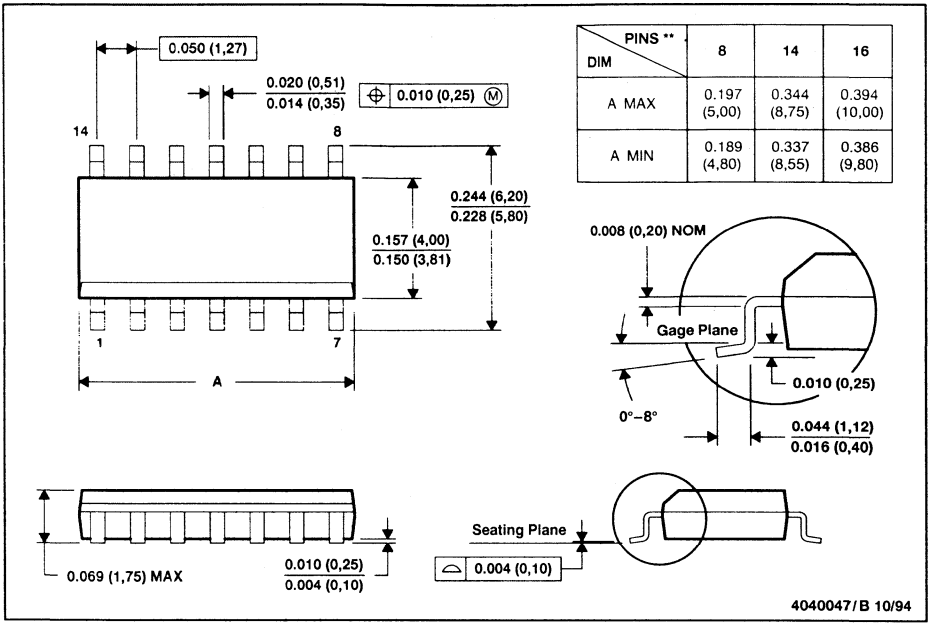
MUST CONTAIN ONE OR TWO LETTERS

LE = Left embossed tape and reel (required for DB and PW packages)
R = Standard tape and reel (optional for D and DW packages)

D (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PIN SHOWN

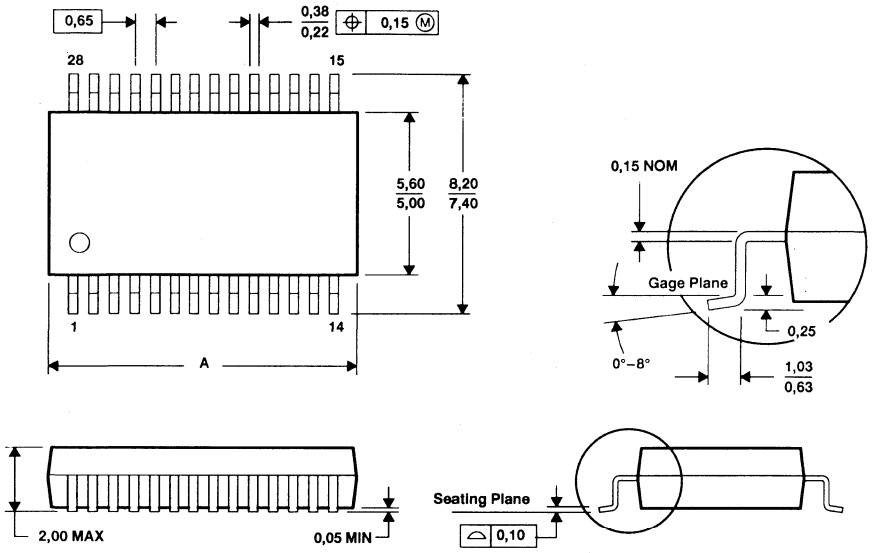


DIM \ PINS **	8	14	16
A MAX	0.197 (5,00)	0.344 (8,75)	0.394 (10,00)
A MIN	0.189 (4,80)	0.337 (8,55)	0.386 (9,80)

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
D. Four center pins are connected to die mount pad.
E. Falls within JEDEC MS-012

DB (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

28 PIN SHOWN



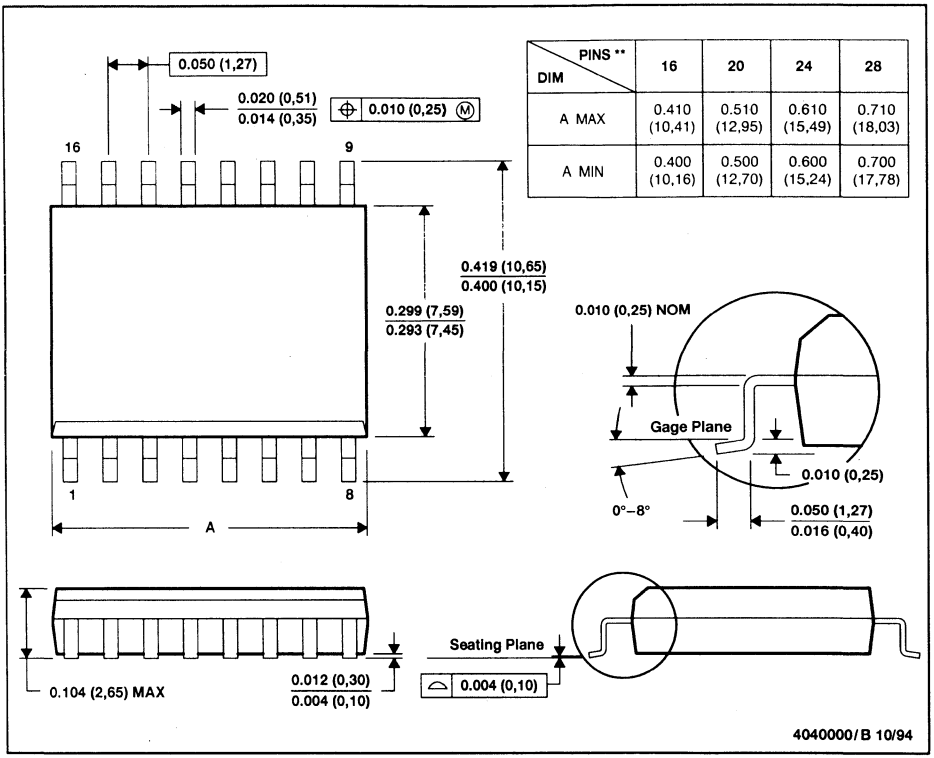
DIM \ PINS **	8	14	16	20	24	28	30	38
A MAX	3,30	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	2,70	5,90	5,90	6,90	7,90	9,90	9,90	12,30

4040065 / C 10/95

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-150

DW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

16 PIN SHOWN



DIM \ PINS **	16	20	24	28
A MAX	0.410 (10,41)	0.510 (12,95)	0.610 (15,49)	0.710 (18,03)
A MIN	0.400 (10,16)	0.500 (12,70)	0.600 (15,24)	0.700 (17,78)

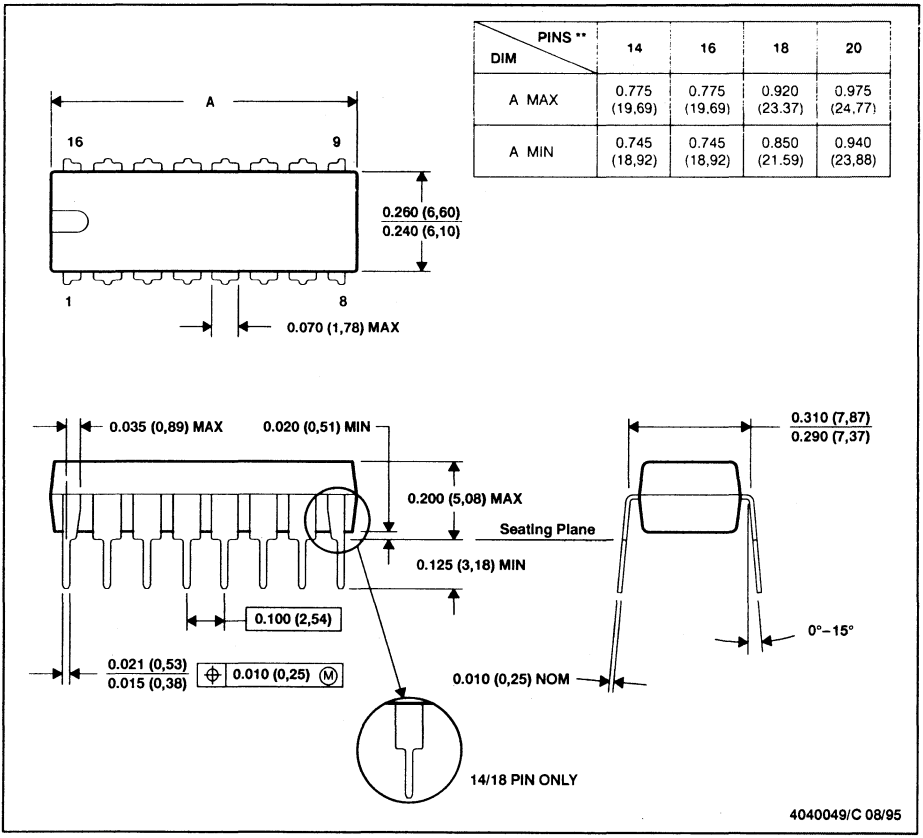
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS-013

MECHANICAL DATA

N (R-PDIP-T)** **PLASTIC DUAL-IN-LINE PACKAGE**

16 PIN SHOWN

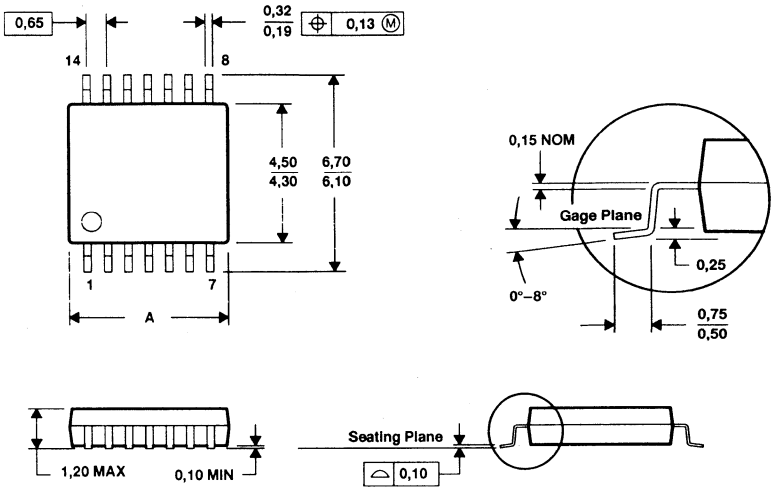
DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23.37)	0.975 (24,77)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21.59)	0.940 (23,88)



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-001 (20 pin package is shorter then MS-001.)

PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PIN SHOWN



DIM \ PINS **	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

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NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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AHC Data Sheets 2
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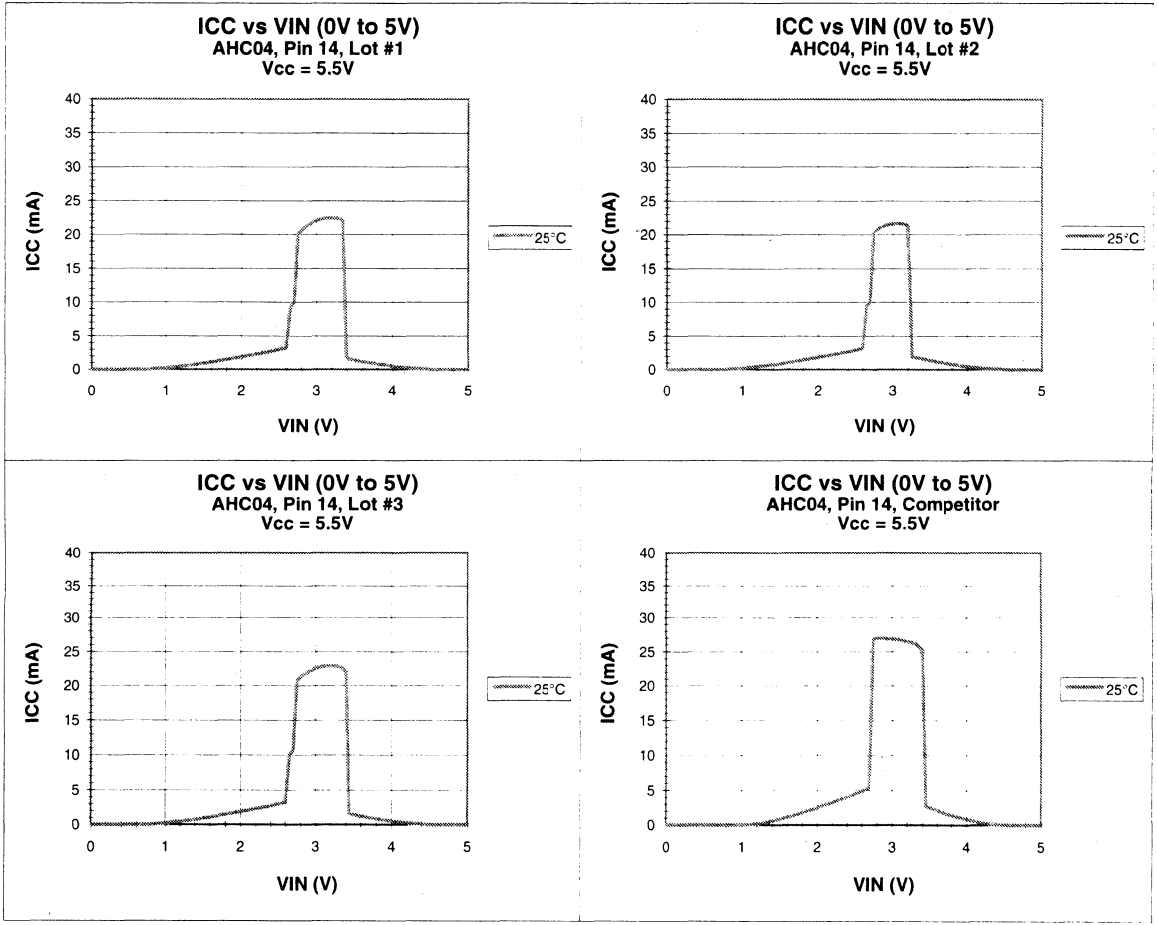
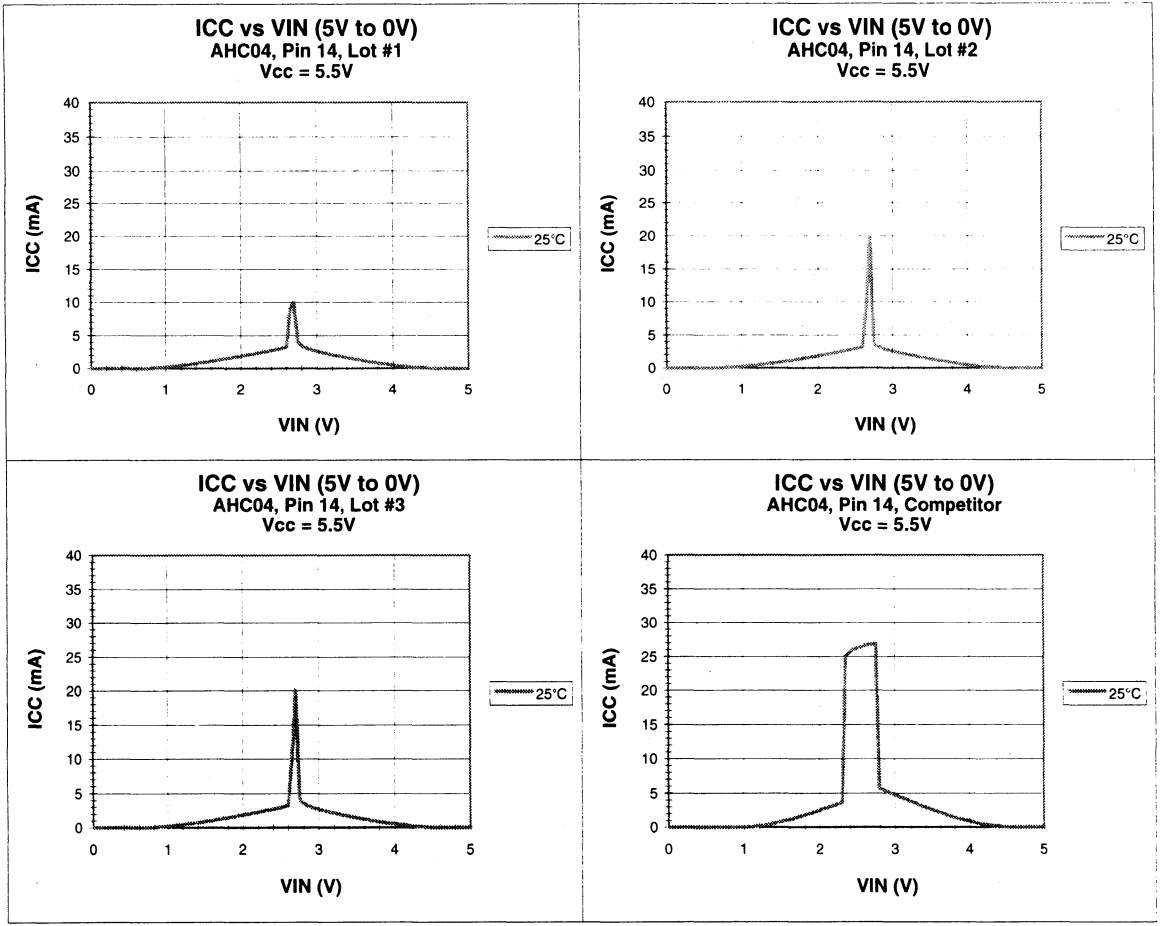
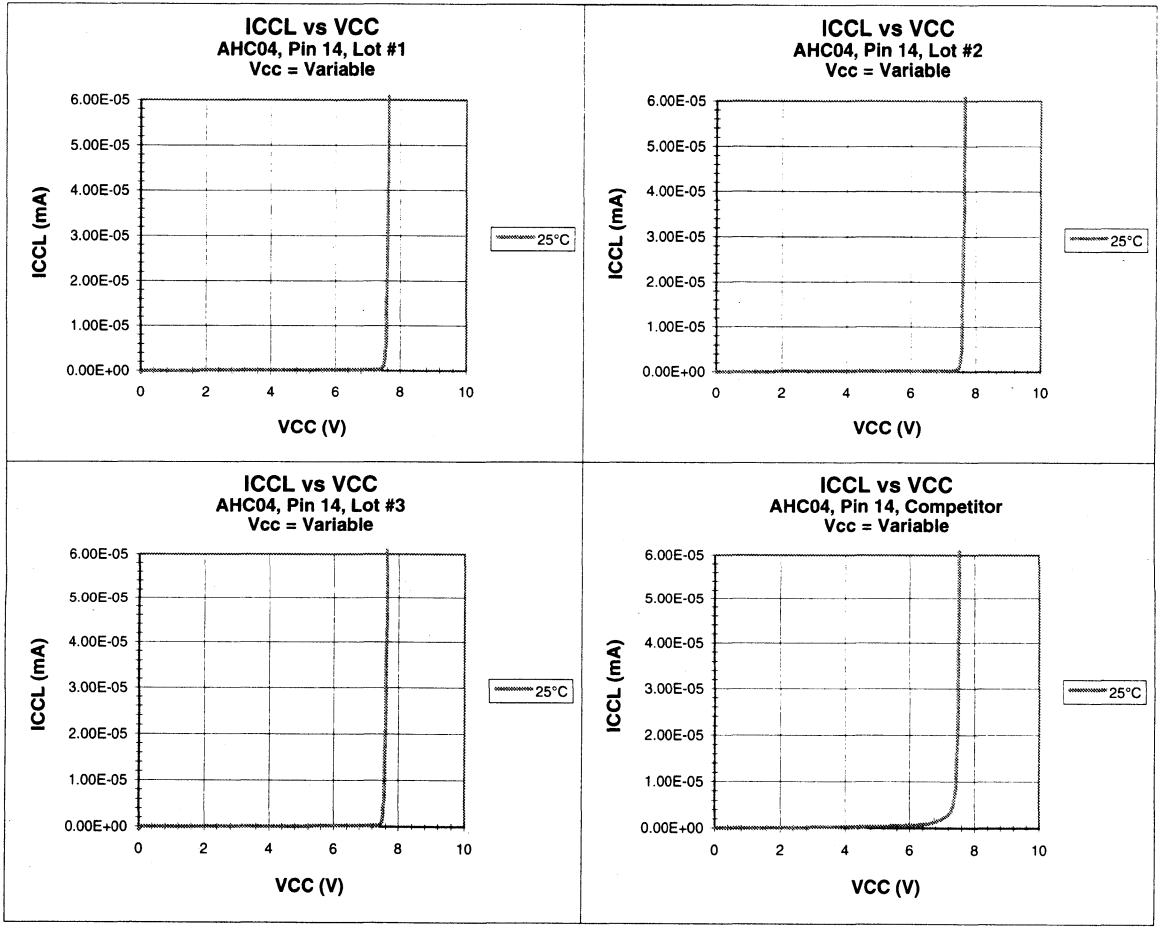
AHC04 Qualification Data A
AHCT04 Qualification Data B
AHC245 Qualification Data C
AHCT245 Qualification Data D

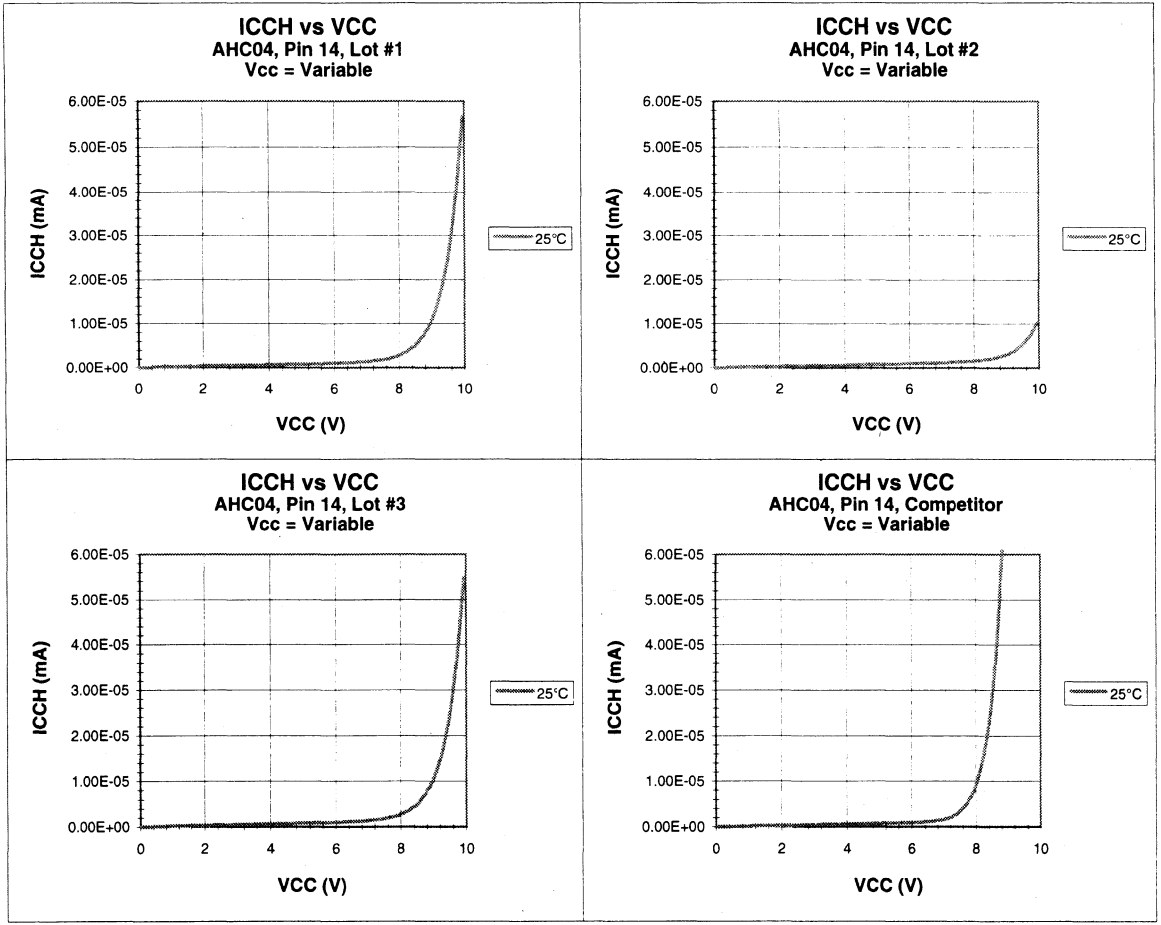
A

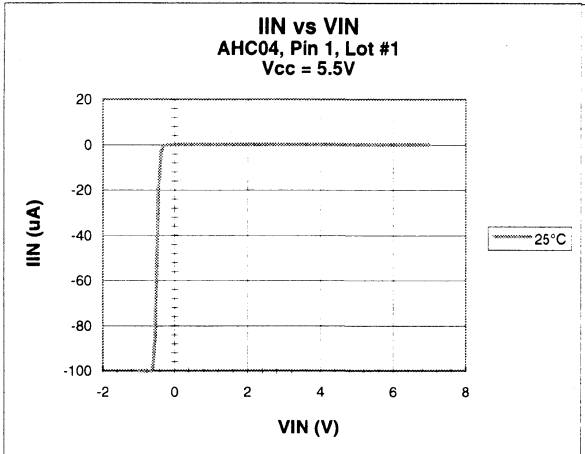
AHC04 Qualification Data

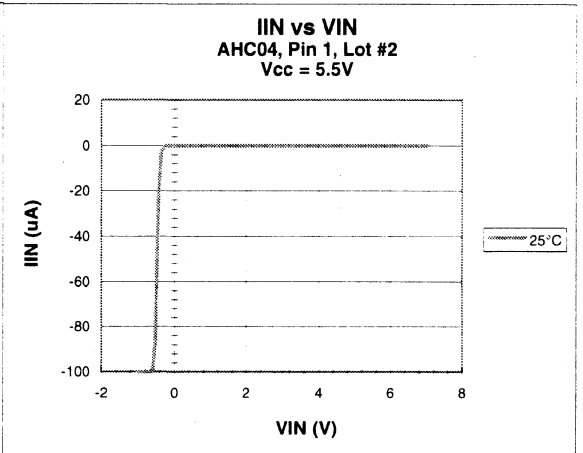

ICC vs VIN (0V to 5V)
AHC04, Pin 14, Lot #1
Vcc = 5.5V
ICC (mA)
VIN (V)
25°C
ICC vs VIN (0V to 5V)
AHC04, Pin 14, Lot #2
Vcc = 5.5V
ICC (mA)
VIN (V)
25°C
ICC vs VIN (0V to 5V)
AHC04, Pin 14, Lot #3
Vcc = 5.5V
ICC (mA)
VIN (V)
25°C
ICC vs VIN (0V to 5V)
AHC04, Pin 14, Competitor
Vcc = 5.5V
ICC (mA)
VIN (V)
25°C

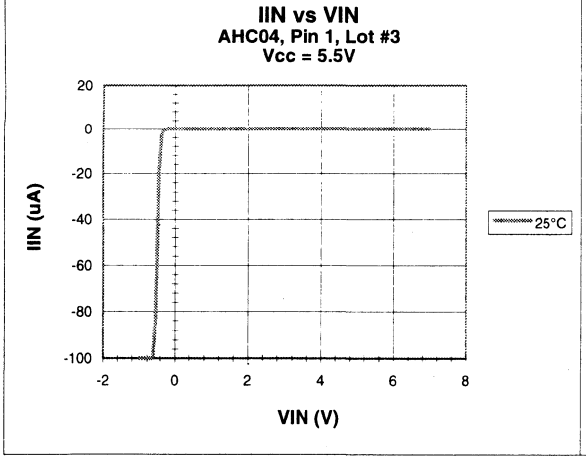

ICC vs VIN (5V to 0V)
AHC04, Pin 14, Lot #1
Vcc = 5.5V
ICC (mA)
VIN (V)
25°C
ICC vs VIN (5V to 0V)
AHC04, Pin 14, Lot #2
Vcc = 5.5V
ICC (mA)
VIN (V)
25°C
ICC vs VIN (5V to 0V)
AHC04, Pin 14, Lot #3
Vcc = 5.5V
ICC (mA)
VIN (V)
25°C
ICC vs VIN (5V to 0V)
AHC04, Pin 14, Competitor
Vcc = 5.5V
ICC (mA)
VIN (V)
25°C

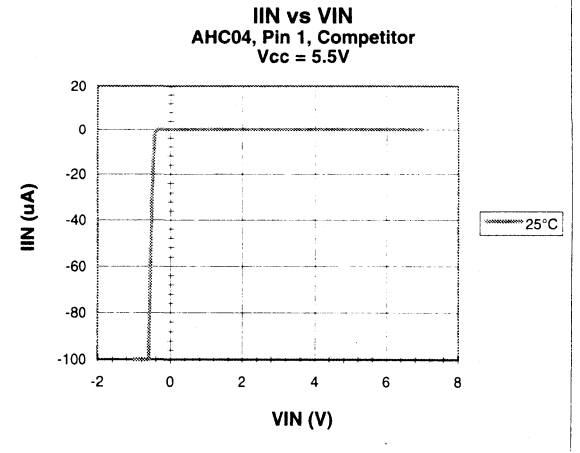

ICCL vs VCC
AHC04, Pin 14, Lot #1
Vcc = Variable
ICCL (mA)
6.00E-05
5.00E-05
4.00E-05
3.00E-05
2.00E-05
1.00E-05
0.00E+00
0
2
4
6
8
10
VCC (V)
25°C
ICCL vs VCC
AHC04, Pin 14, Lot #2
Vcc = Variable
ICCL (mA)
6.00E-05
5.00E-05
4.00E-05
3.00E-05
2.00E-05
1.00E-05
0.00E+00
0
2
4
6
8
10
VCC (V)
25°C
ICCL vs VCC
AHC04, Pin 14, Lot #3
Vcc = Variable
ICCL (mA)
6.00E-05
5.00E-05
4.00E-05
3.00E-05
2.00E-05
1.00E-05
0.00E+00
0
2
4
6
8
10
VCC (V)
25°C
ICCL vs VCC
AHC04, Pin 14, Competitor
Vcc = Variable
ICCL (mA)
6.00E-05
5.00E-05
4.00E-05
3.00E-05
2.00E-05
1.00E-05
0.00E+00
0
2
4
6
8
10
VCC (V)
25°C

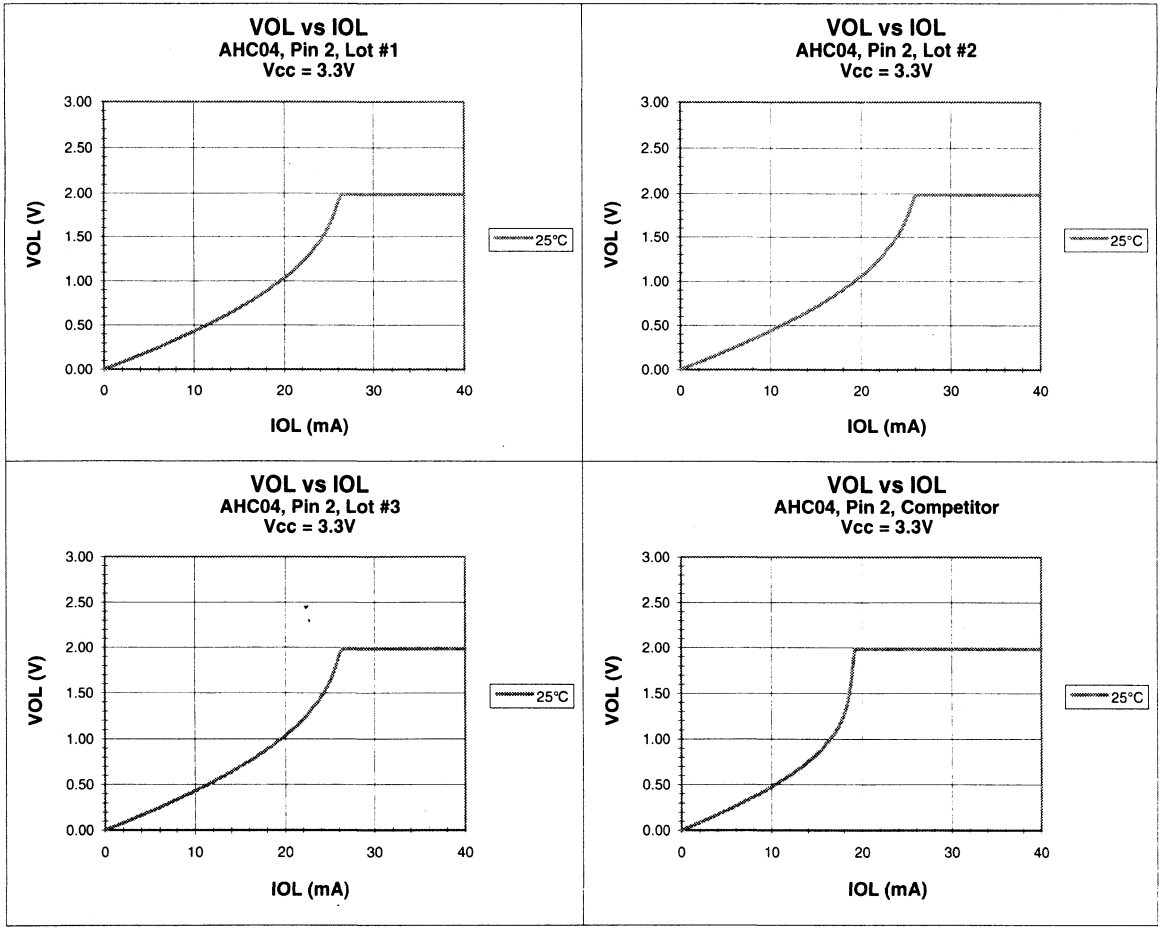

ICCH vs VCC
AHC04, Pin 14, Lot #1
Vcc = Variable
ICCH (mA)
6.00E-05
5.00E-05
4.00E-05
3.00E-05
2.00E-05
1.00E-05
0.00E+00
0
2
4
6
8
10
VCC (V)
25°C
ICCH vs VCC
AHC04, Pin 14, Lot #2
Vcc = Variable
ICCH (mA)
6.00E-05
5.00E-05
4.00E-05
3.00E-05
2.00E-05
1.00E-05
0.00E+00
0
2
4
6
8
10
VCC (V)
25°C
ICCH vs VCC
AHC04, Pin 14, Lot #3
Vcc = Variable
ICCH (mA)
6.00E-05
5.00E-05
4.00E-05
3.00E-05
2.00E-05
1.00E-05
0.00E+00
0
2
4
6
8
10
VCC (V)
25°C
ICCH vs VCC
AHC04, Pin 14, Competitor
Vcc = Variable
ICCH (mA)
6.00E-05
5.00E-05
4.00E-05
3.00E-05
2.00E-05
1.00E-05
0.00E+00
0
2
4
6
8
10
VCC (V)
25°C

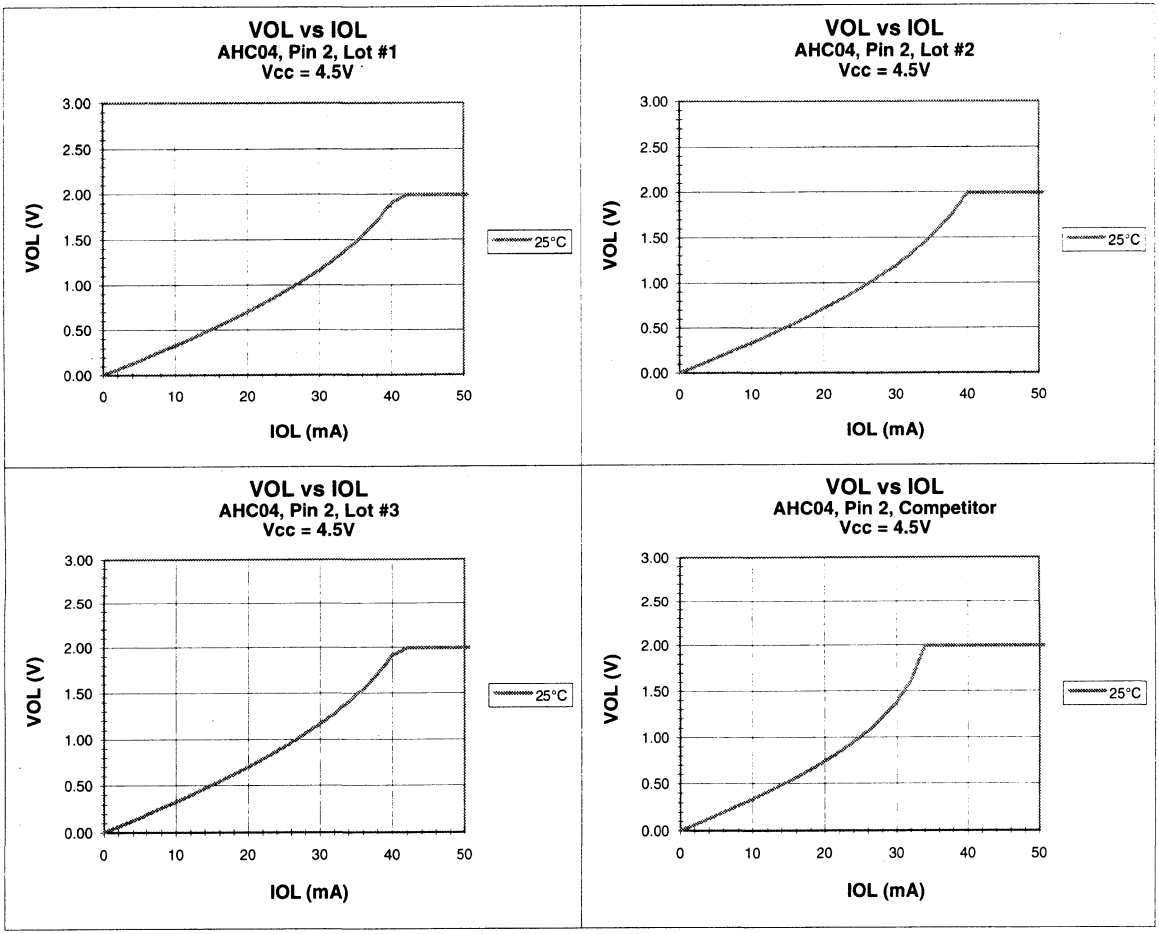

IIN vs VIN
AHC04, Pin 1, Lot #1
Vcc = 5.5V
IIN (uA)
20
0
-20
-40
-60
-80
-100
-2
0
2
4
6
8
VIN (V)
25°C

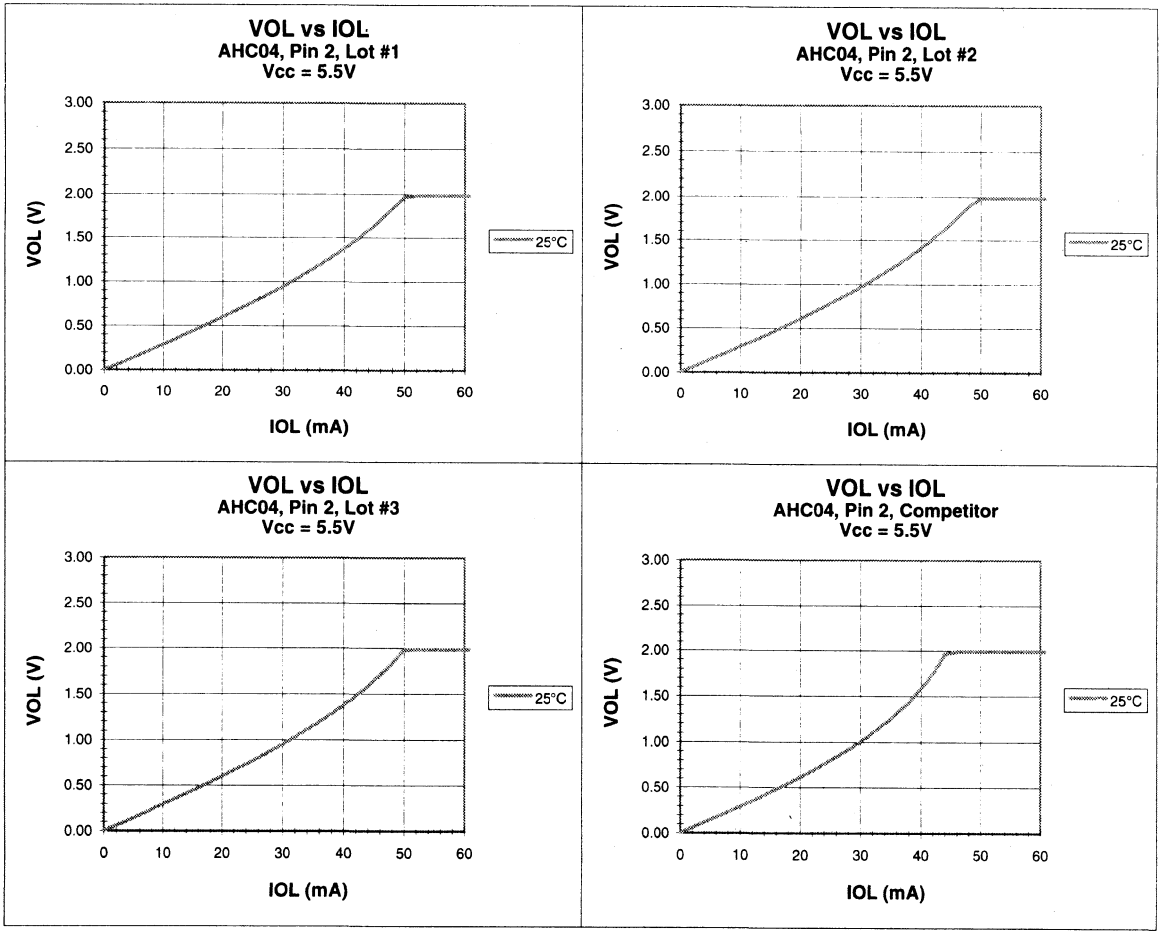

IIN vs VIN
AHC04, Pin 1, Lot #2
Vcc = 5.5V
IIN (uA)
20
0
-20
-40
-60
-80
-100
-2
0
2
4
6
8
VIN (V)
25°C

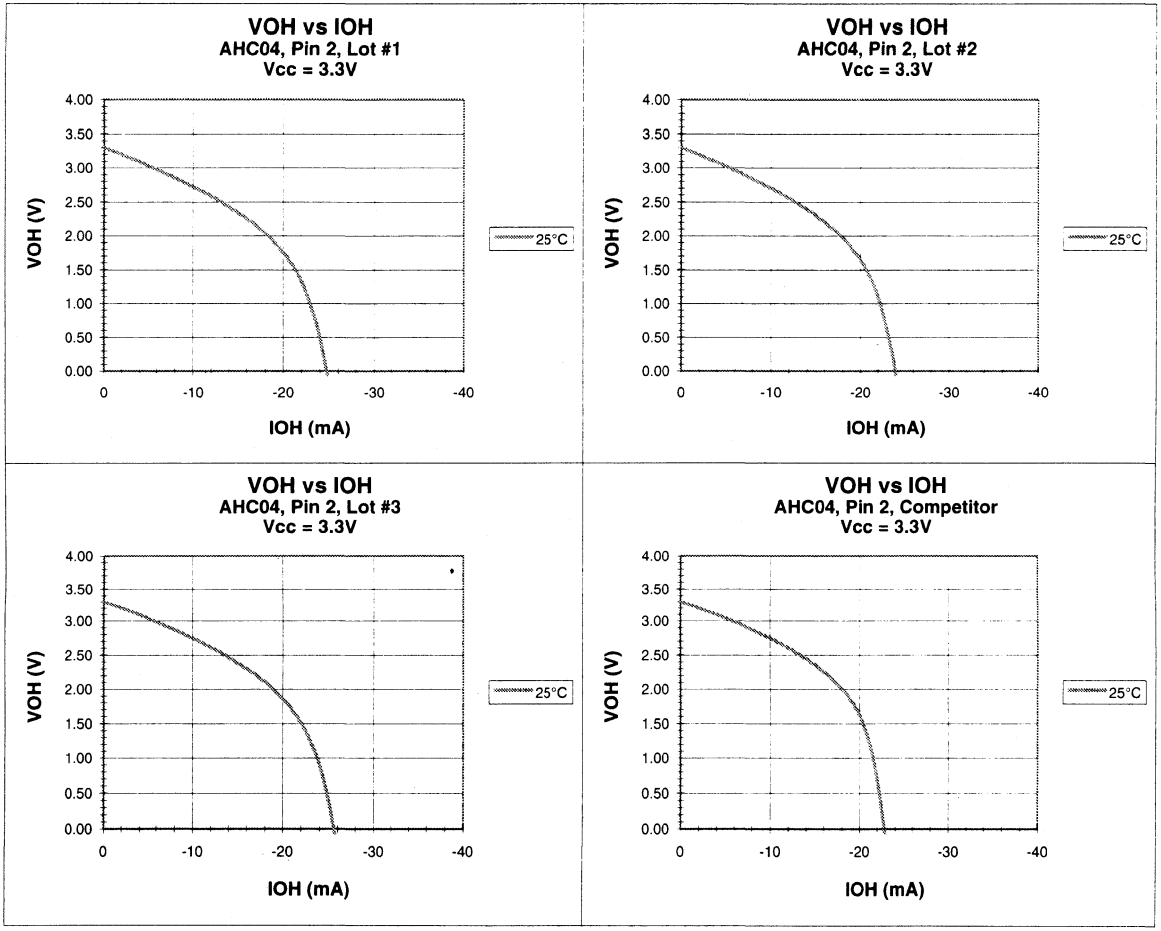

IIN vs VIN
AHC04, Pin 1, Lot #3
Vcc = 5.5V
IIN (uA)
20
0
-20
-40
-60
-80
-100
-2
0
2
4
6
8
VIN (V)
25°C

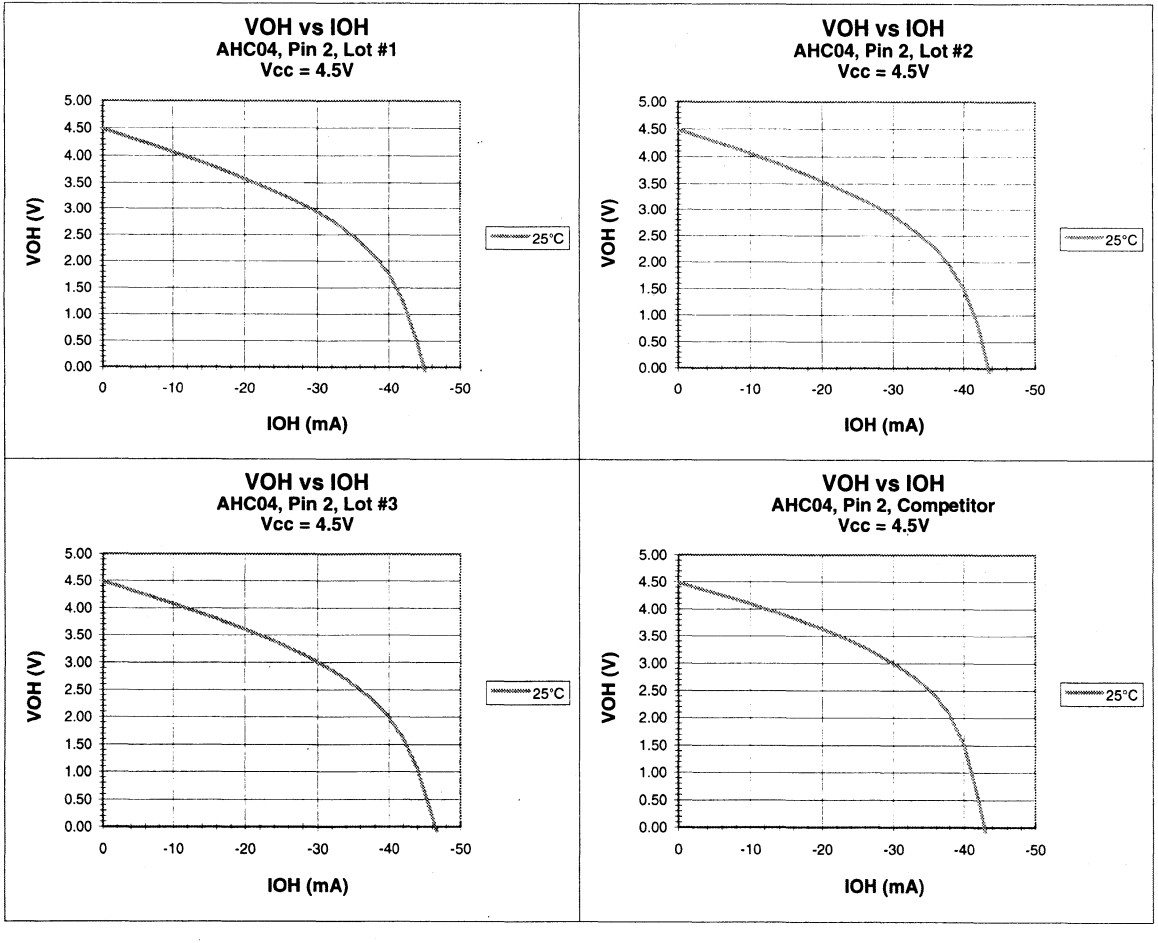

IIN vs VIN
AHC04, Pin 1, Competitor
Vcc = 5.5V
IIN (uA)
20
0
-20
-40
-60
-80
-100
-2
0
2
4
6
8
VIN (V)
25°C

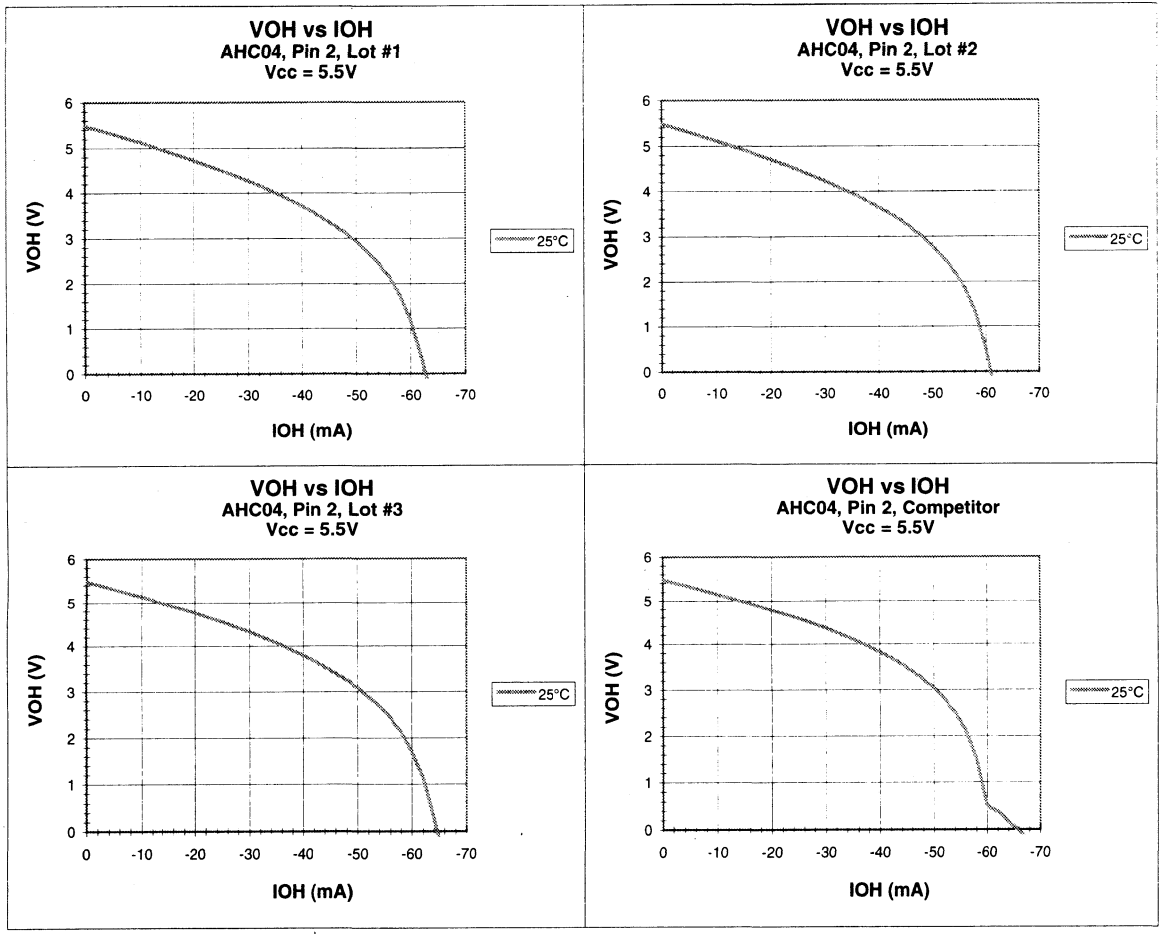

VOL vs IOL
AHC04, Pin 2, Lot #1
Vcc = 3.3V
VOL (V)
3.00
2.50
2.00
1.50
1.00
0.50
0.00
0
10
20
30
40
IOL (mA)
25°C
VOL vs IOL
AHC04, Pin 2, Lot #2
Vcc = 3.3V
VOL (V)
IOL (mA)
25°C
VOL vs IOL
AHC04, Pin 2, Lot #3
Vcc = 3.3V
VOL (V)
IOL (mA)
25°C
VOL vs IOL
AHC04, Pin 2, Competitor
Vcc = 3.3V
VOL (V)
IOL (mA)
25°C

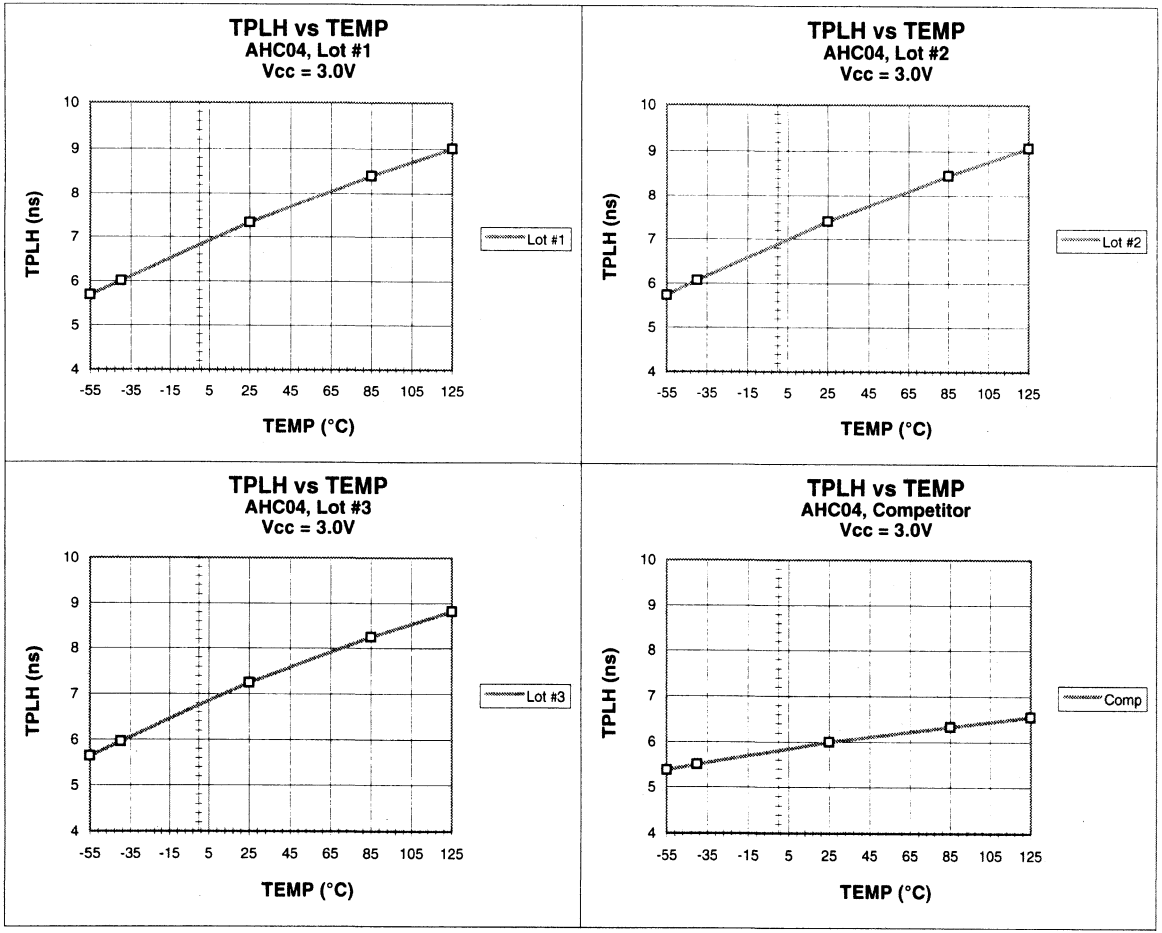

VOL vs IOL
AHC04, Pin 2, Lot #1
Vcc = 4.5V
VOL (V)
3.00
2.50
2.00
1.50
1.00
0.50
0.00
0
10
20
30
40
50
IOL (mA)
25°C
VOL vs IOL
AHC04, Pin 2, Lot #2
Vcc = 4.5V
VOL (V)
IOL (mA)
25°C
VOL vs IOL
AHC04, Pin 2, Lot #3
Vcc = 4.5V
VOL (V)
IOL (mA)
25°C
VOL vs IOL
AHC04, Pin 2, Competitor
Vcc = 4.5V
VOL (V)
IOL (mA)
25°C

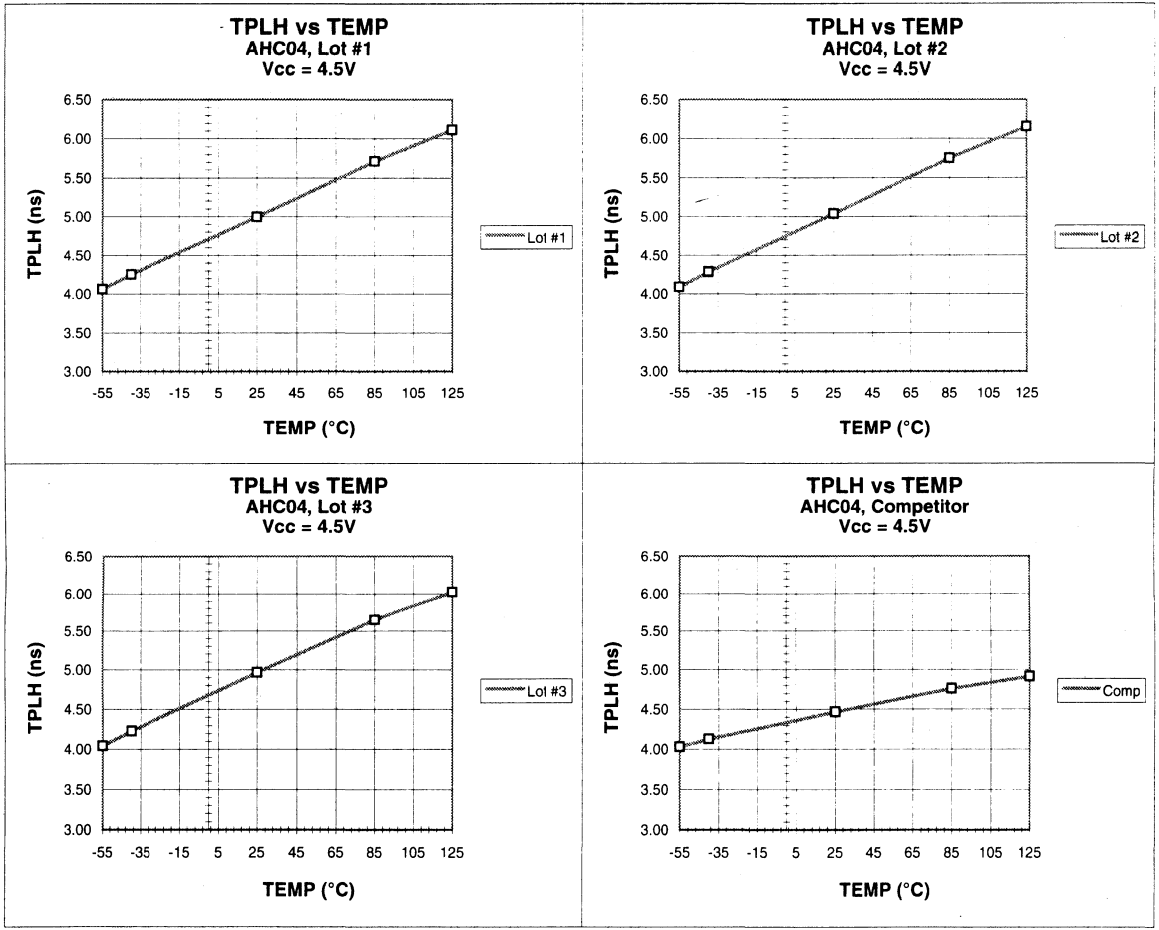

VOL vs IOL
AHC04, Pin 2, Lot #1
Vcc = 5.5V
VOL (V)
3.00
2.50
2.00
1.50
1.00
0.50
0.00
0
10
20
30
40
50
60
IOL (mA)
25°C
VOL vs IOL
AHC04, Pin 2, Lot #2
Vcc = 5.5V
VOL (V)
IOL (mA)
25°C
VOL vs IOL
AHC04, Pin 2, Lot #3
Vcc = 5.5V
VOL (V)
IOL (mA)
25°C
VOL vs IOL
AHC04, Pin 2, Competitor
Vcc = 5.5V
VOL (V)
IOL (mA)
25°C

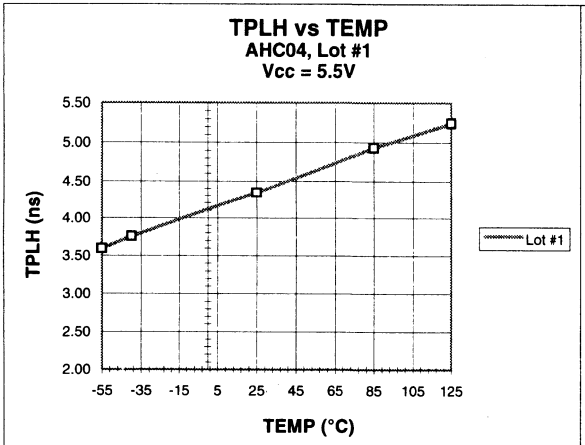

VOH vs IOH
AHC04, Pin 2, Lot #1
Vcc = 3.3V
VOH (V)
4.00
3.50
3.00
2.50
2.00
1.50
1.00
0.50
0.00
0
-10
-20
-30
-40
IOH (mA)
25°C
VOH vs IOH
AHC04, Pin 2, Lot #2
Vcc = 3.3V
VOH (V)
IOH (mA)
25°C
VOH vs IOH
AHC04, Pin 2, Lot #3
Vcc = 3.3V
VOH (V)
IOH (mA)
25°C
VOH vs IOH
AHC04, Pin 2, Competitor
Vcc = 3.3V
VOH (V)
IOH (mA)
25°C

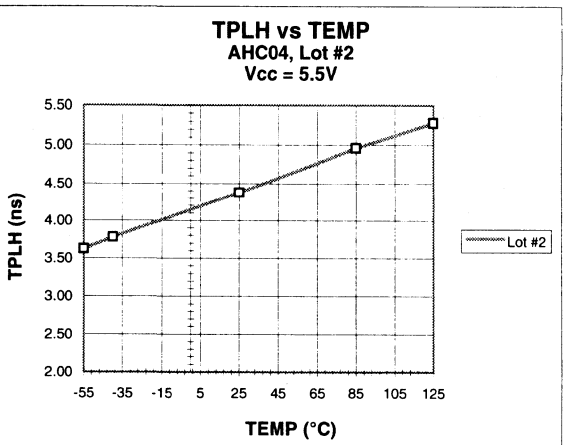

VOH vs IOH
AHC04, Pin 2, Lot #1
Vcc = 4.5V
VOH (V)
5.00
4.50
4.00
3.50
3.00
2.50
2.00
1.50
1.00
0.50
0.00
0
-10
-20
-30
-40
-50
IOH (mA)
25°C
VOH vs IOH
AHC04, Pin 2, Lot #2
Vcc = 4.5V
VOH (V)
IOH (mA)
25°C
VOH vs IOH
AHC04, Pin 2, Lot #3
Vcc = 4.5V
VOH (V)
IOH (mA)
25°C
VOH vs IOH
AHC04, Pin 2, Competitor
Vcc = 4.5V
VOH (V)
IOH (mA)
25°C

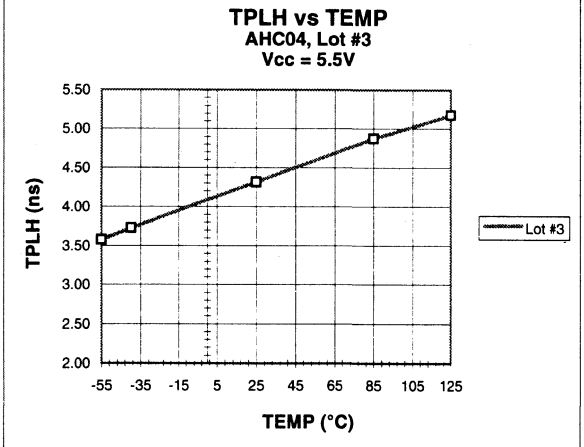

VOH vs IOH
AHC04, Pin 2, Lot #1
Vcc = 5.5V
VOH (V)
IOH (mA)
25°C
VOH vs IOH
AHC04, Pin 2, Lot #2
Vcc = 5.5V
VOH (V)
IOH (mA)
25°C
VOH vs IOH
AHC04, Pin 2, Lot #3
Vcc = 5.5V
VOH (V)
IOH (mA)
25°C
VOH vs IOH
AHC04, Pin 2, Competitor
Vcc = 5.5V
VOH (V)
IOH (mA)
25°C

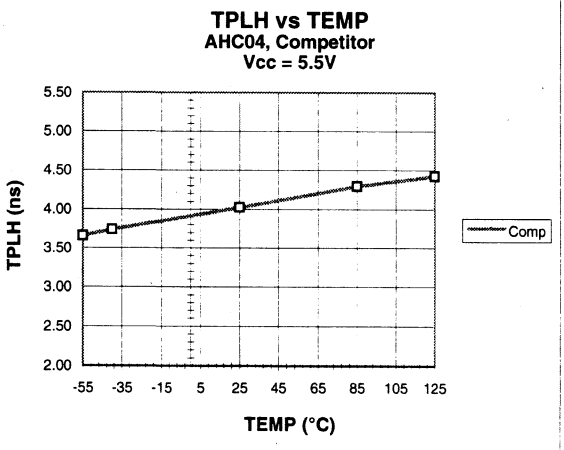

TPLH vs TEMP
AHC04, Lot #1
Vcc = 3.0V
TPLH (ns)
10
9
8
7
6
5
4
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Lot #1
TPLH vs TEMP
AHC04, Lot #2
Vcc = 3.0V
TPLH (ns)
10
9
8
7
6
5
4
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Lot #2
TPLH vs TEMP
AHC04, Lot #3
Vcc = 3.0V
TPLH (ns)
10
9
8
7
6
5
4
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Lot #3
TPLH vs TEMP
AHC04, Competitor
Vcc = 3.0V
TPLH (ns)
10
9
8
7
6
5
4
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Comp

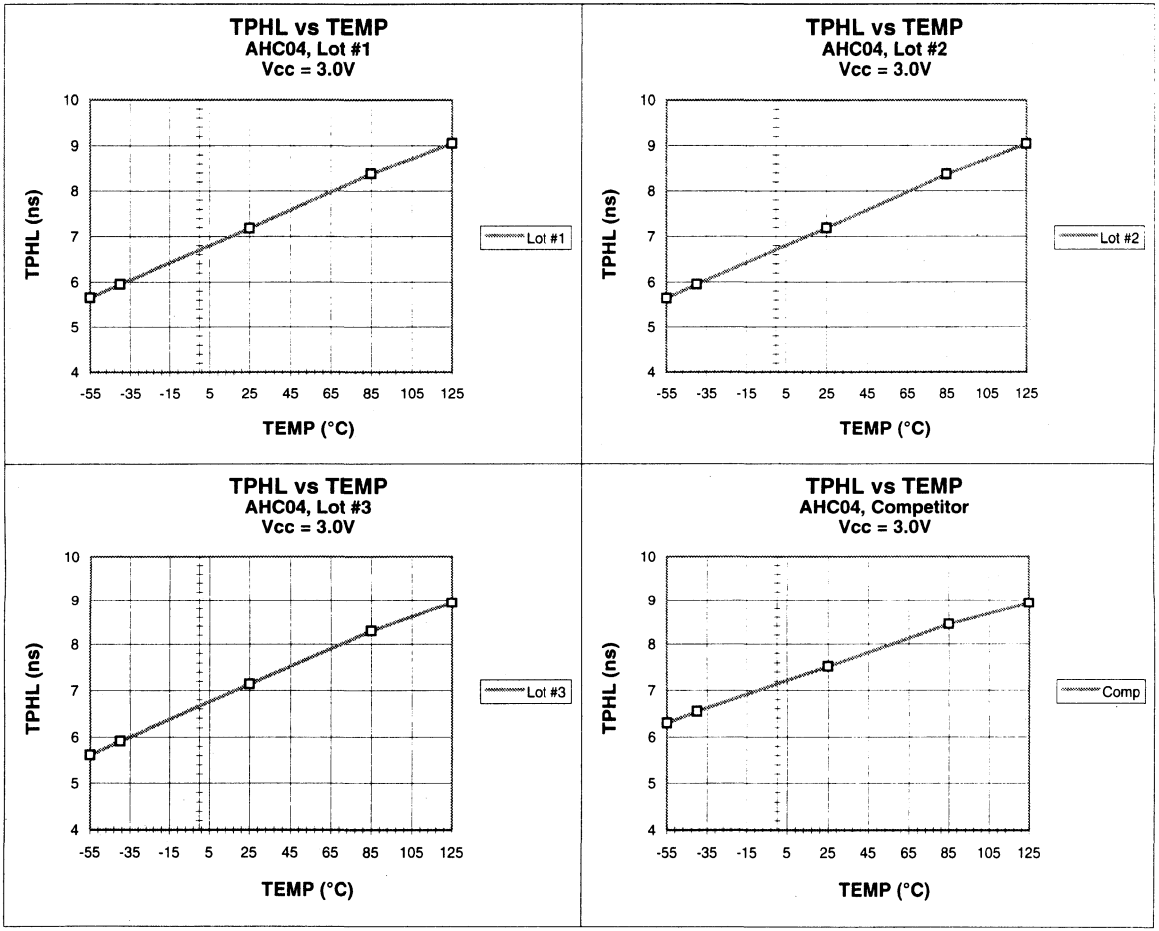

TPLH vs TEMP
AHC04, Lot #1
Vcc = 4.5V
TPLH (ns)
6.50
6.00
5.50
5.00
4.50
4.00
3.50
3.00
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Lot #1
TPLH vs TEMP
AHC04, Lot #2
Vcc = 4.5V
TPLH (ns)
6.50
6.00
5.50
5.00
4.50
4.00
3.50
3.00
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Lot #2
TPLH vs TEMP
AHC04, Lot #3
Vcc = 4.5V
TPLH (ns)
6.50
6.00
5.50
5.00
4.50
4.00
3.50
3.00
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Lot #3
TPLH vs TEMP
AHC04, Competitor
Vcc = 4.5V
TPLH (ns)
6.50
6.00
5.50
5.00
4.50
4.00
3.50
3.00
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Comp

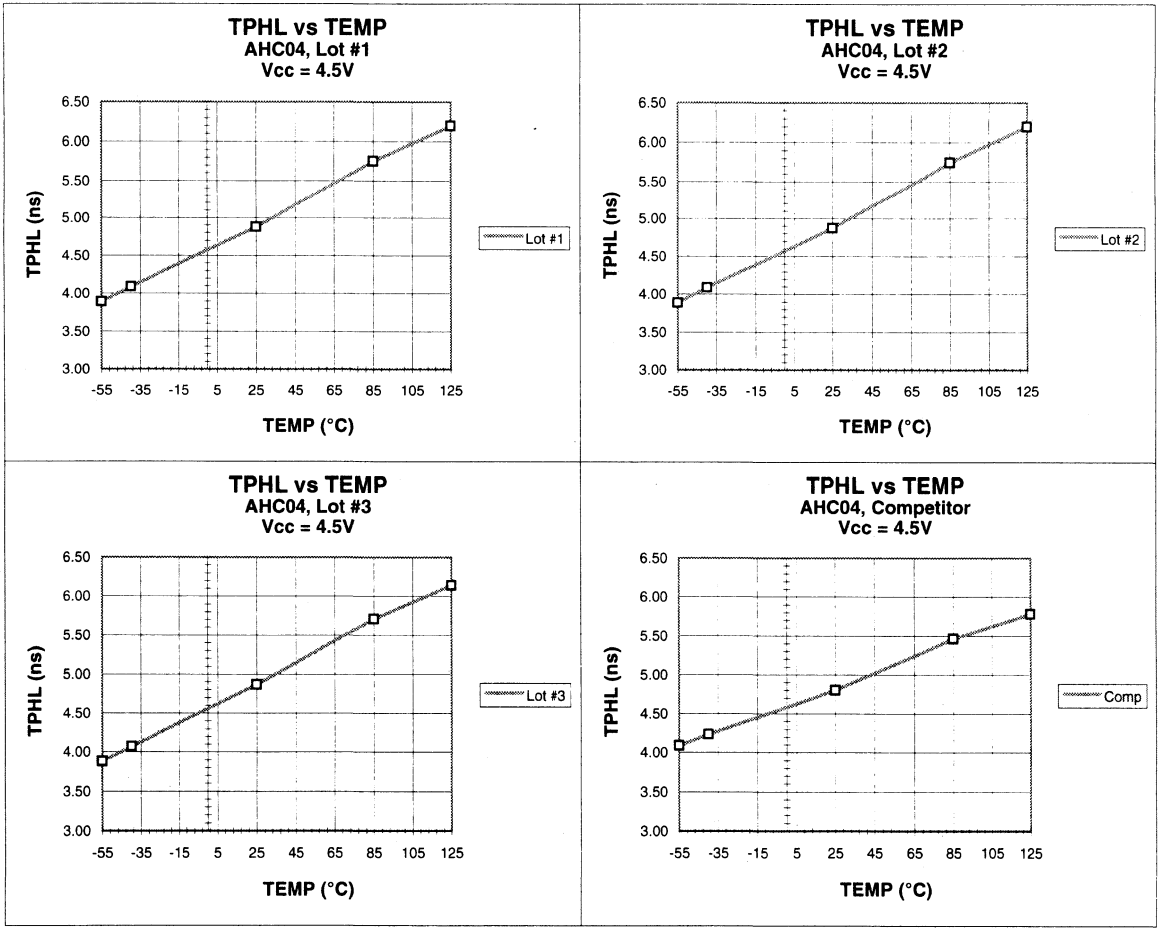

TPLH vs TEMP
AHC04, Lot #1
Vcc = 5.5V
TPLH (ns)
5.50
5.00
4.50
4.00
3.50
3.00
2.50
2.00
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Lot #1

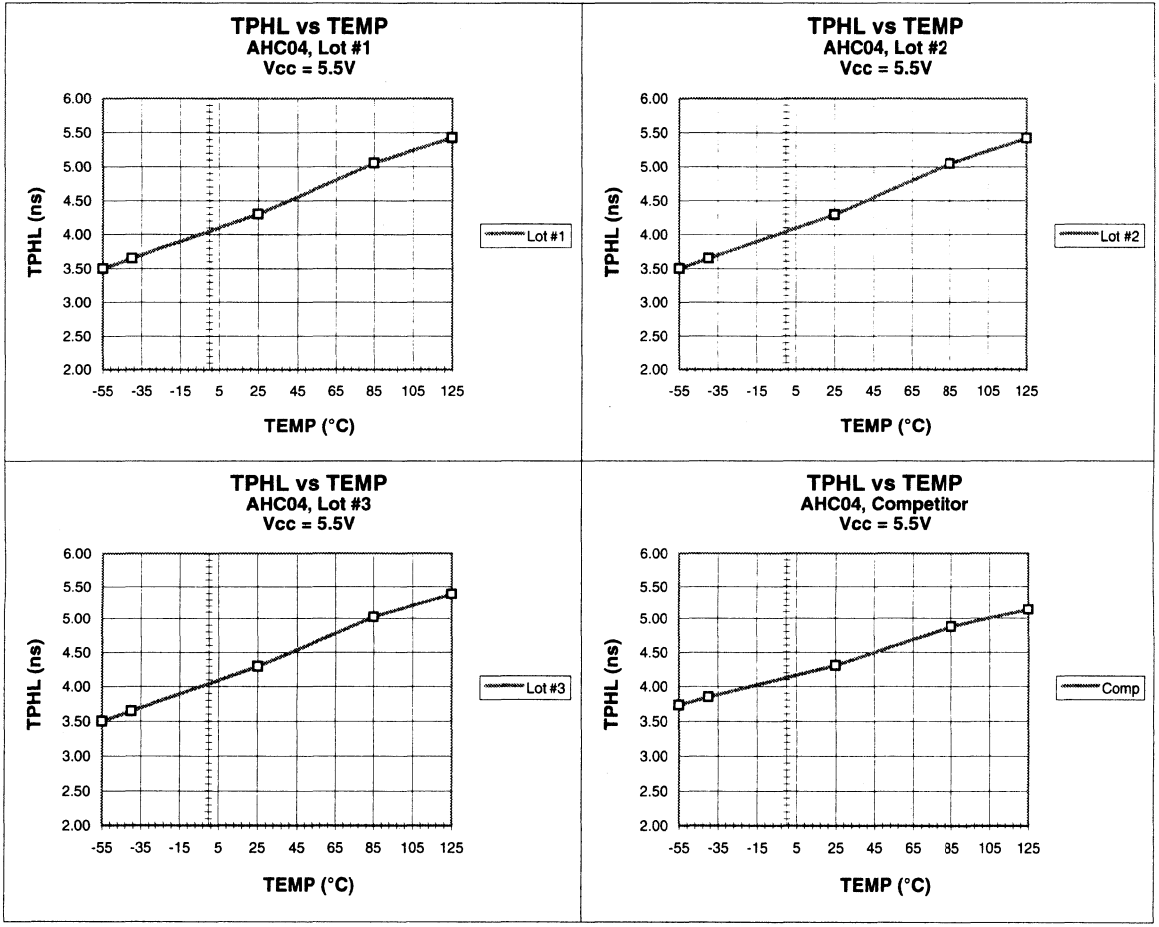

TPLH vs TEMP
AHC04, Lot #2
Vcc = 5.5V
TPLH (ns)
5.50
5.00
4.50
4.00
3.50
3.00
2.50
2.00
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Lot #2


TPLH vs TEMP
AHC04, Lot #3
Vcc = 5.5V
TPLH (ns)
5.50
5.00
4.50
4.00
3.50
3.00
2.50
2.00
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Lot #3


TPLH vs TEMP
AHC04, Competitor
Vcc = 5.5V
TPLH (ns)
5.50
5.00
4.50
4.00
3.50
3.00
2.50
2.00
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Comp

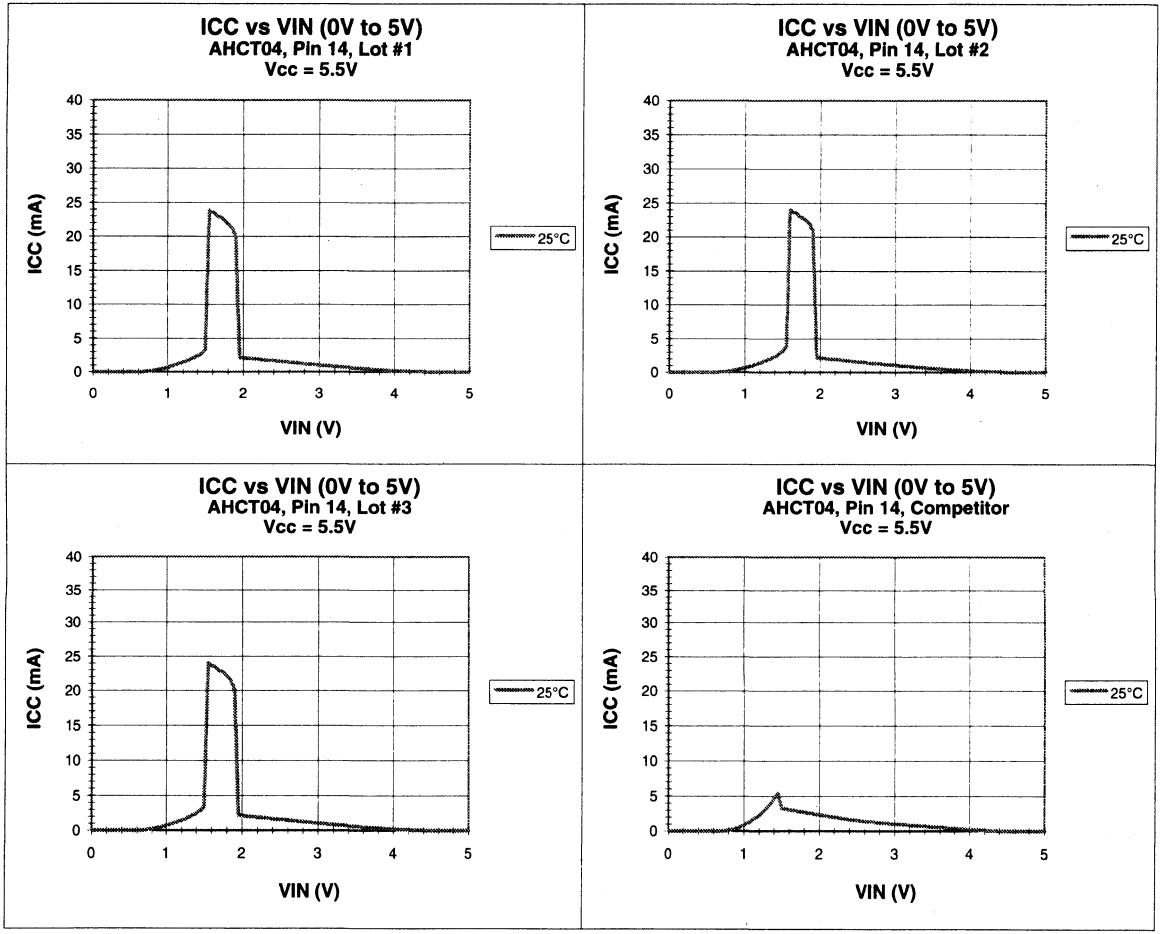

TPHL vs TEMP
AHC04, Lot #1
Vcc = 3.0V
TPHL (ns)
10
9
8
7
6
5
4
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Lot #1
TPHL vs TEMP
AHC04, Lot #2
Vcc = 3.0V
TPHL (ns)
10
9
8
7
6
5
4
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Lot #2
TPHL vs TEMP
AHC04, Lot #3
Vcc = 3.0V
TPHL (ns)
10
9
8
7
6
5
4
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Lot #3
TPHL vs TEMP
AHC04, Competitor
Vcc = 3.0V
TPHL (ns)
10
9
8
7
6
5
4
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Comp

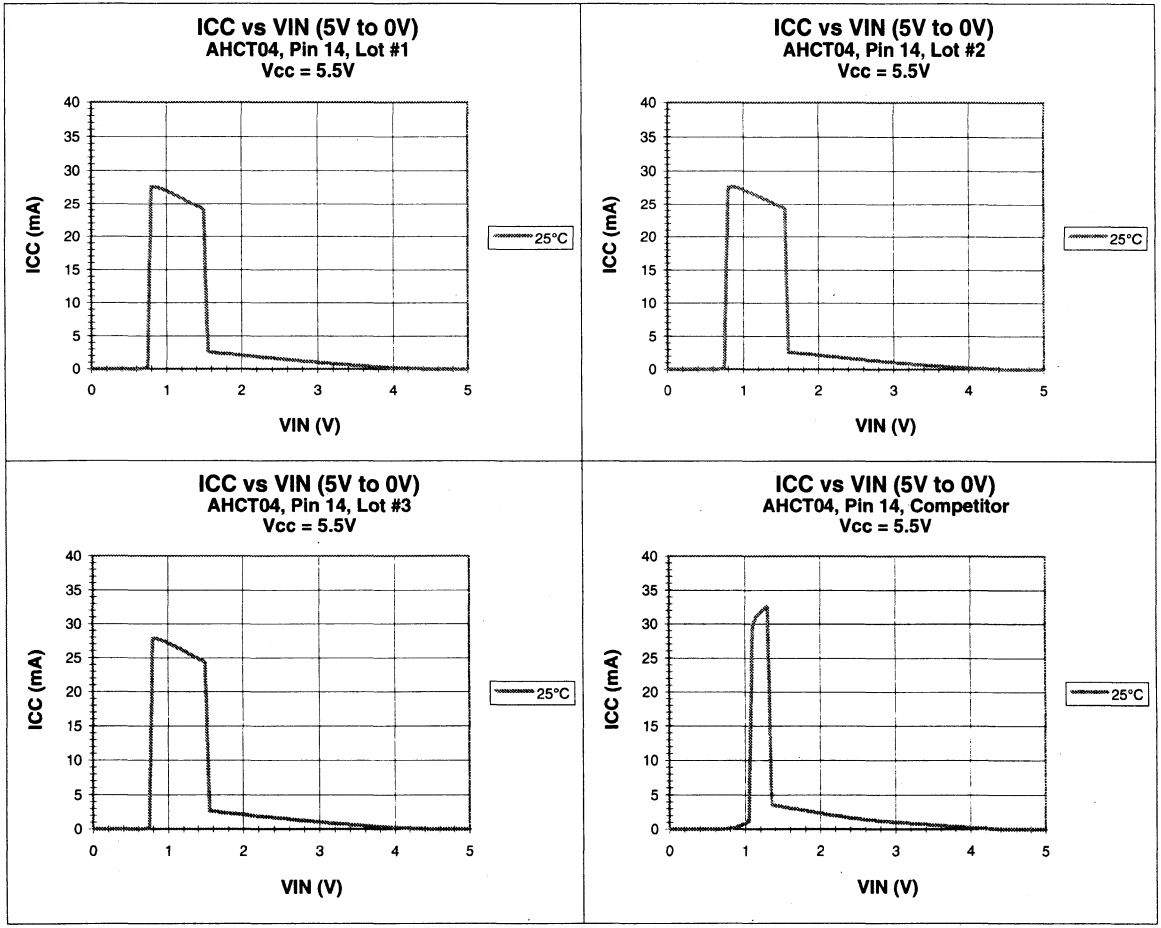

TPHL vs TEMP
AHC04, Lot #1
Vcc = 4.5V
TPHL (ns)
6.50
6.00
5.50
5.00
4.50
4.00
3.50
3.00
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Lot #1
TPHL vs TEMP
AHC04, Lot #2
Vcc = 4.5V
TPHL (ns)
6.50
6.00
5.50
5.00
4.50
4.00
3.50
3.00
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Lot #2
TPHL vs TEMP
AHC04, Lot #3
Vcc = 4.5V
TPHL (ns)
6.50
6.00
5.50
5.00
4.50
4.00
3.50
3.00
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Lot #3
TPHL vs TEMP
AHC04, Competitor
Vcc = 4.5V
TPHL (ns)
6.50
6.00
5.50
5.00
4.50
4.00
3.50
3.00
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Comp

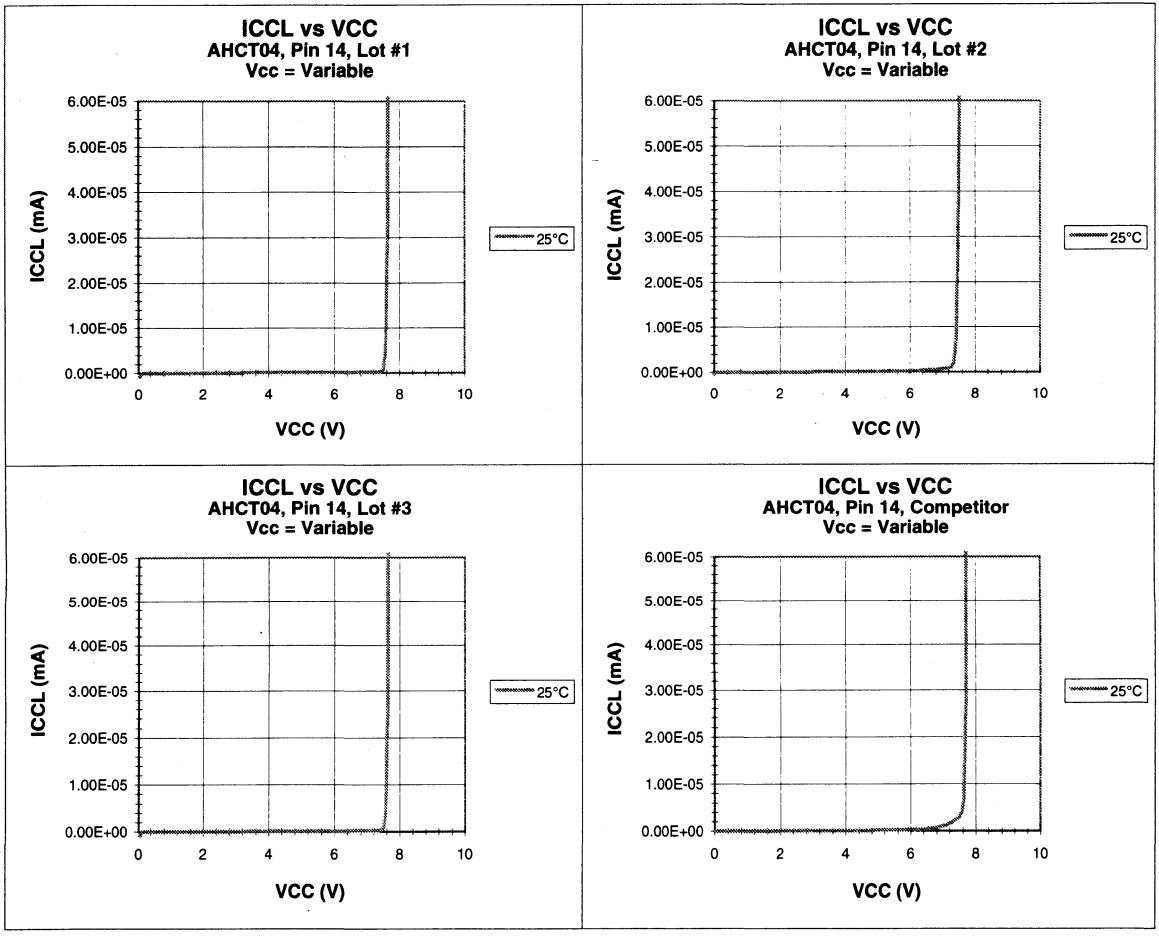

TPHL vs TEMP
AHC04, Lot #1
Vcc = 5.5V
TPHL (ns)
6.00
5.50
5.00
4.50
4.00
3.50
3.00
2.50
2.00
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Lot #1
TPHL vs TEMP
AHC04, Lot #2
Vcc = 5.5V
TPHL (ns)
6.00
5.50
5.00
4.50
4.00
3.50
3.00
2.50
2.00
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Lot #2
TPHL vs TEMP
AHC04, Lot #3
Vcc = 5.5V
TPHL (ns)
6.00
5.50
5.00
4.50
4.00
3.50
3.00
2.50
2.00
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Lot #3
TPHL vs TEMP
AHC04, Competitor
Vcc = 5.5V
TPHL (ns)
6.00
5.50
5.00
4.50
4.00
3.50
3.00
2.50
2.00
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Comp

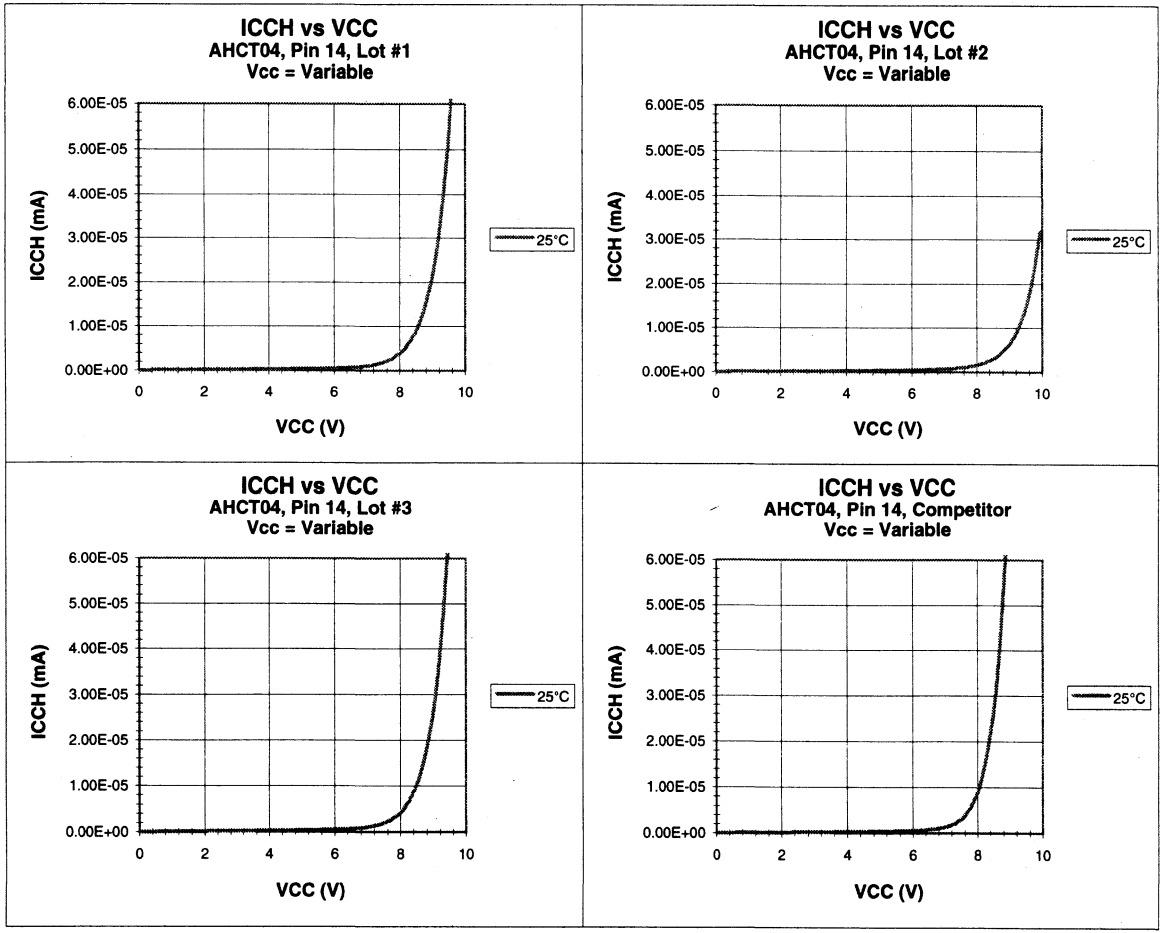
General Information 1
AHC Data Sheets 2
AHCT Data Sheets 3
Mechanical Data 4
AHC04 Qualification Data A
AHCT04 Qualification Data B
AHC245 Qualification Data C
AHCT245 Qualification Data D

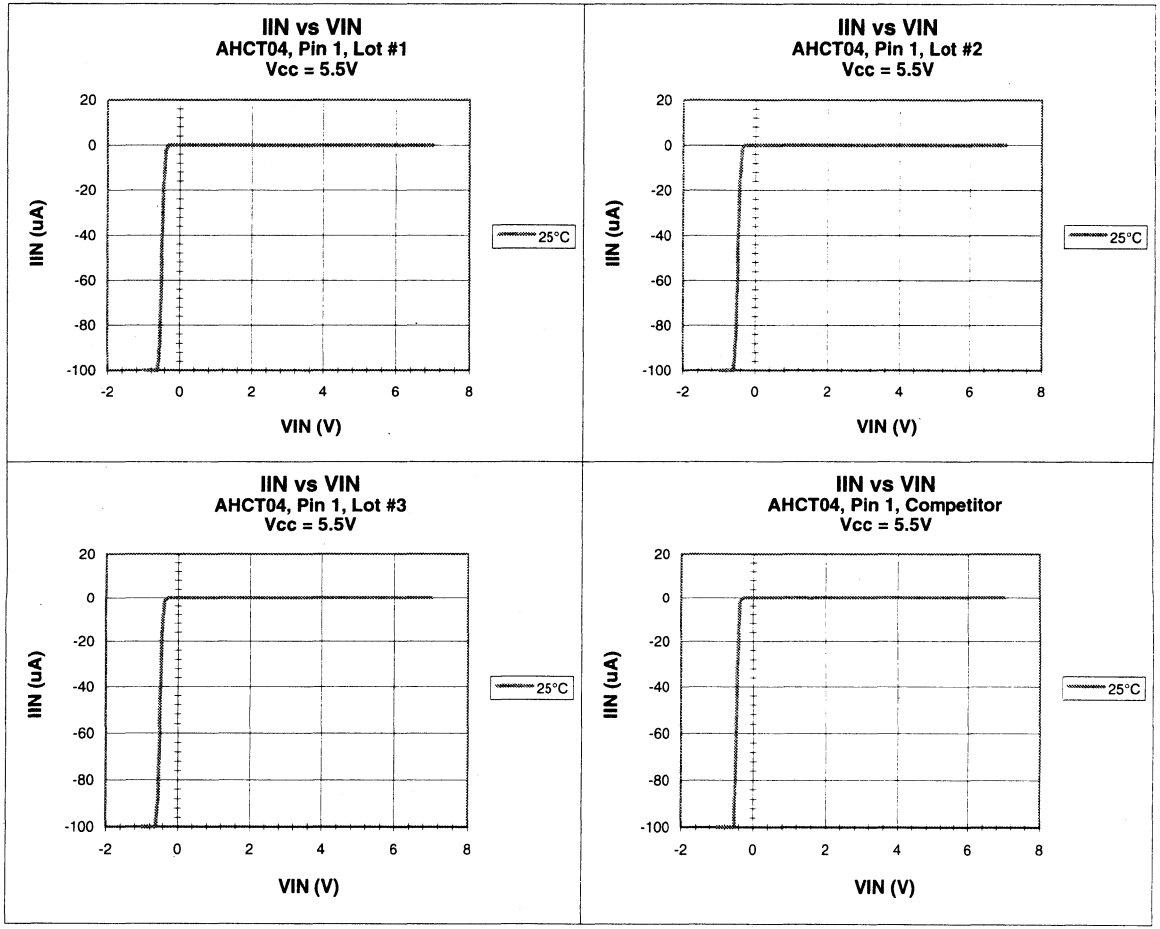
B AHCT04 Qualification Data

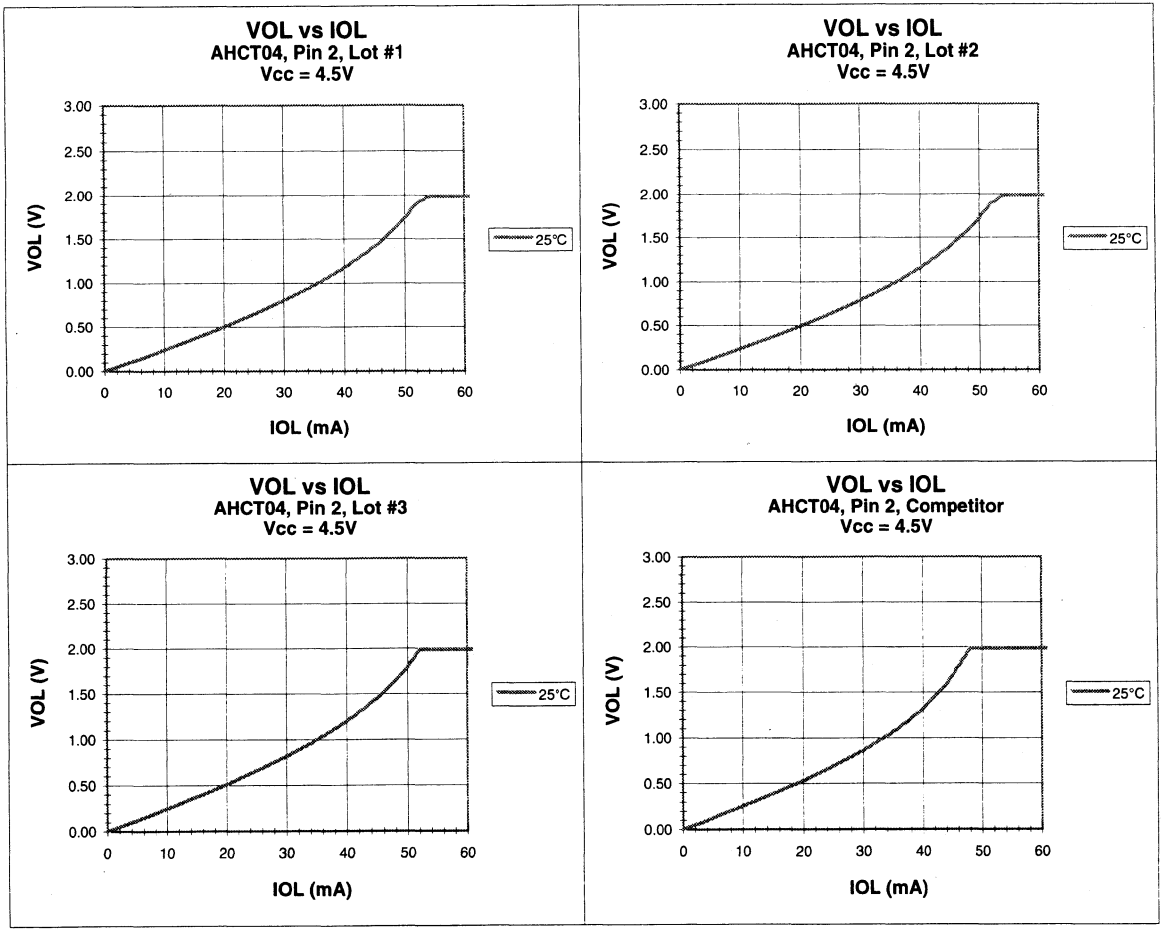

ICC vs VIN (0V to 5V)
AHCT04, Pin 14, Lot #1
Vcc = 5.5V
ICC (mA)
VIN (V)
25°C
ICC vs VIN (0V to 5V)
AHCT04, Pin 14, Lot #2
Vcc = 5.5V
ICC (mA)
VIN (V)
25°C
ICC vs VIN (0V to 5V)
AHCT04, Pin 14, Lot #3
Vcc = 5.5V
ICC (mA)
VIN (V)
25°C
ICC vs VIN (0V to 5V)
AHCT04, Pin 14, Competitor
Vcc = 5.5V
ICC (mA)
VIN (V)
25°C

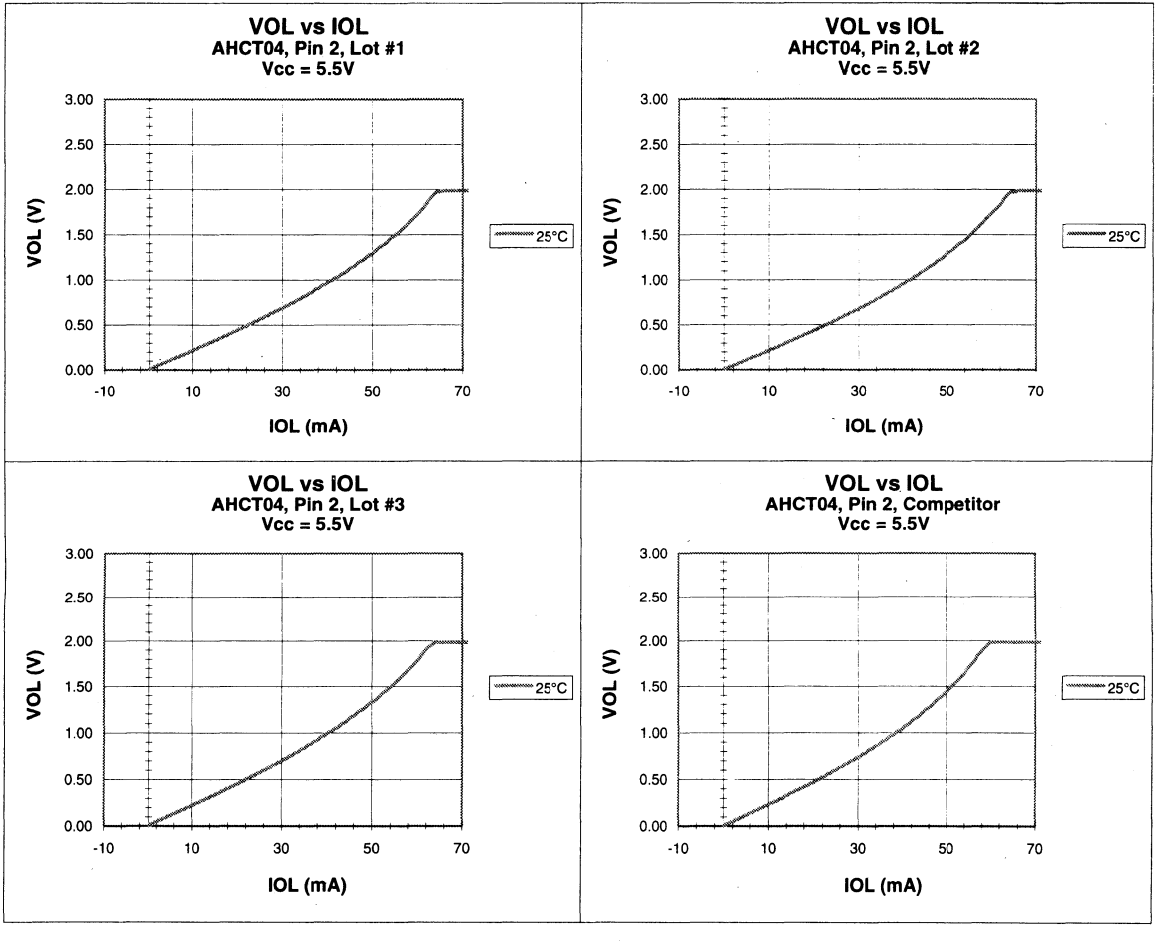

ICC vs VIN (5V to 0V)
AHCT04, Pin 14, Lot #1
Vcc = 5.5V
ICC (mA)
VIN (V)
25°C
ICC vs VIN (5V to 0V)
AHCT04, Pin 14, Lot #2
Vcc = 5.5V
ICC (mA)
VIN (V)
25°C
ICC vs VIN (5V to 0V)
AHCT04, Pin 14, Lot #3
Vcc = 5.5V
ICC (mA)
VIN (V)
25°C
ICC vs VIN (5V to 0V)
AHCT04, Pin 14, Competitor
Vcc = 5.5V
ICC (mA)
VIN (V)
25°C

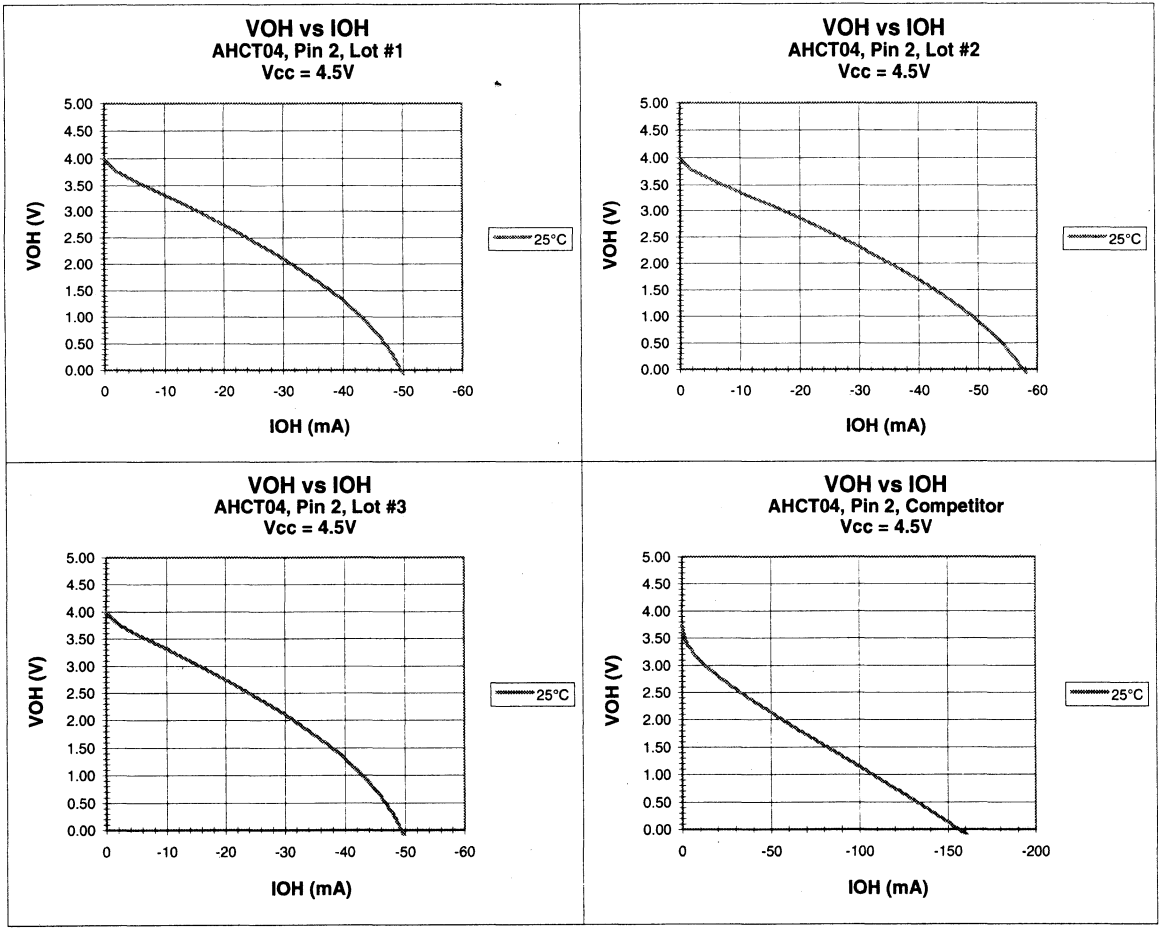

ICCL vs VCC
AHCT04, Pin 14, Lot #1
Vcc = Variable
ICCL (mA)
6.00E-05
5.00E-05
4.00E-05
3.00E-05
2.00E-05
1.00E-05
0.00E+00
0
2
4
6
8
10
VCC (V)
25°C
ICCL vs VCC
AHCT04, Pin 14, Lot #2
Vcc = Variable
ICCL (mA)
6.00E-05
5.00E-05
4.00E-05
3.00E-05
2.00E-05
1.00E-05
0.00E+00
0
2
4
6
8
10
VCC (V)
25°C
ICCL vs VCC
AHCT04, Pin 14, Lot #3
Vcc = Variable
ICCL (mA)
6.00E-05
5.00E-05
4.00E-05
3.00E-05
2.00E-05
1.00E-05
0.00E+00
0
2
4
6
8
10
VCC (V)
25°C
ICCL vs VCC
AHCT04, Pin 14, Competitor
Vcc = Variable
ICCL (mA)
6.00E-05
5.00E-05
4.00E-05
3.00E-05
2.00E-05
1.00E-05
0.00E+00
0
2
4
6
8
10
VCC (V)
25°C

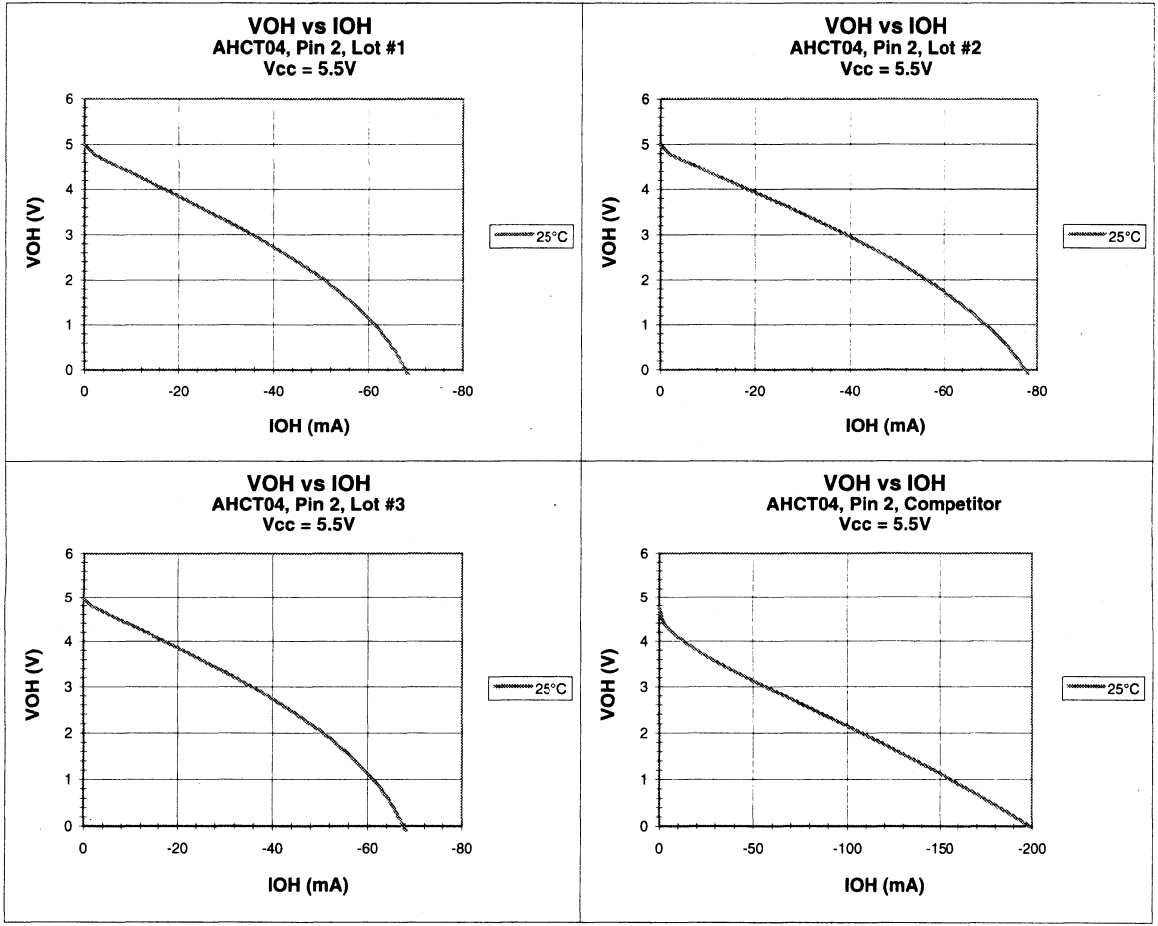

ICCH vs VCC
AHCT04, Pin 14, Lot #1
Vcc = Variable
ICCH (mA)
6.00E-05
5.00E-05
4.00E-05
3.00E-05
2.00E-05
1.00E-05
0.00E+00
0
2
4
6
8
10
VCC (V)
25°C
ICCH vs VCC
AHCT04, Pin 14, Lot #2
Vcc = Variable
ICCH (mA)
6.00E-05
5.00E-05
4.00E-05
3.00E-05
2.00E-05
1.00E-05
0.00E+00
0
2
4
6
8
10
VCC (V)
25°C
ICCH vs VCC
AHCT04, Pin 14, Lot #3
Vcc = Variable
ICCH (mA)
6.00E-05
5.00E-05
4.00E-05
3.00E-05
2.00E-05
1.00E-05
0.00E+00
0
2
4
6
8
10
VCC (V)
25°C
ICCH vs VCC
AHCT04, Pin 14, Competitor
Vcc = Variable
ICCH (mA)
6.00E-05
5.00E-05
4.00E-05
3.00E-05
2.00E-05
1.00E-05
0.00E+00
0
2
4
6
8
10
VCC (V)
25°C

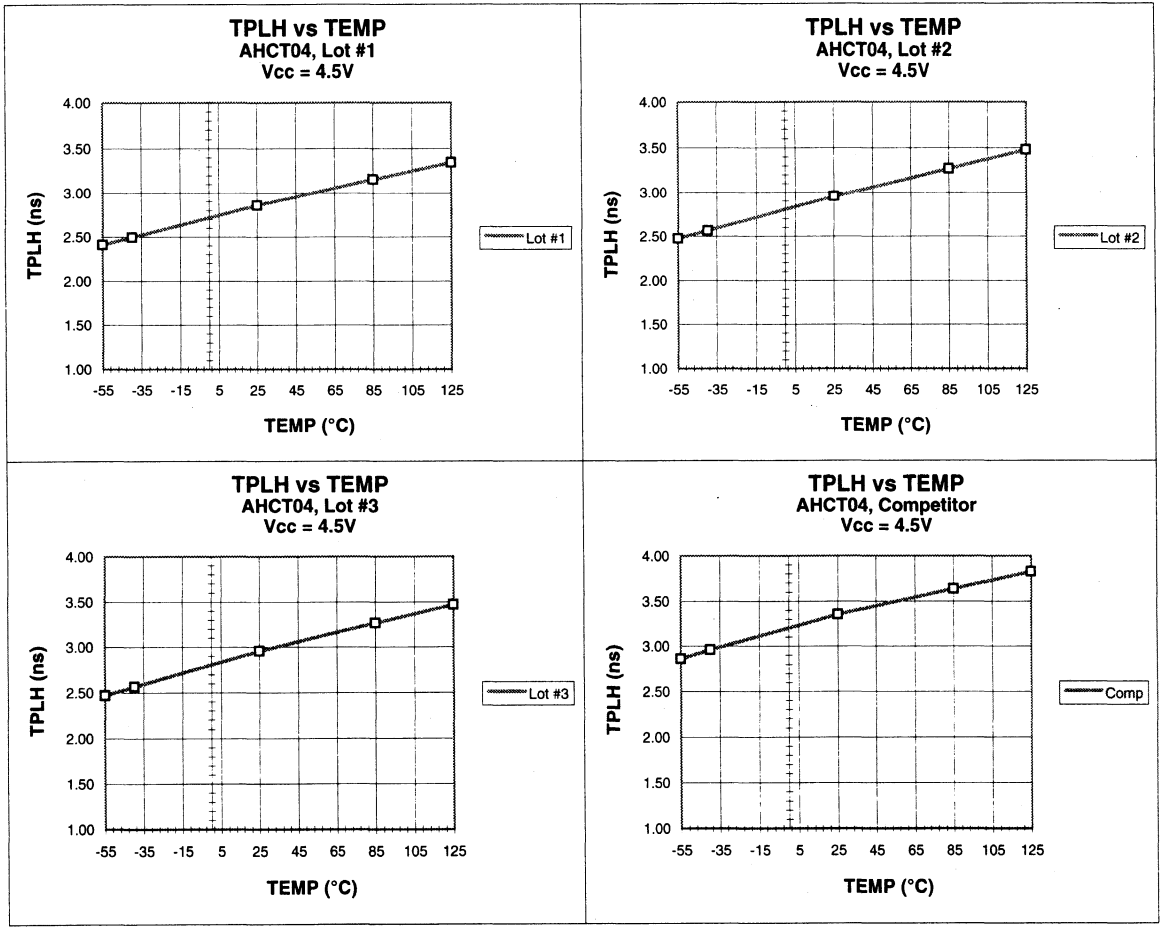

IIN vs VIN
AHCT04, Pin 1, Lot #1
Vcc = 5.5V
IIN (uA)
20
0
-20
-40
-60
-80
-100
-2
0
2
4
6
8
VIN (V)
25°C
IIN vs VIN
AHCT04, Pin 1, Lot #2
Vcc = 5.5V
IIN (uA)
VIN (V)
25°C
IIN vs VIN
AHCT04, Pin 1, Lot #3
Vcc = 5.5V
IIN (uA)
VIN (V)
25°C
IIN vs VIN
AHCT04, Pin 1, Competitor
Vcc = 5.5V
IIN (uA)
VIN (V)
25°C

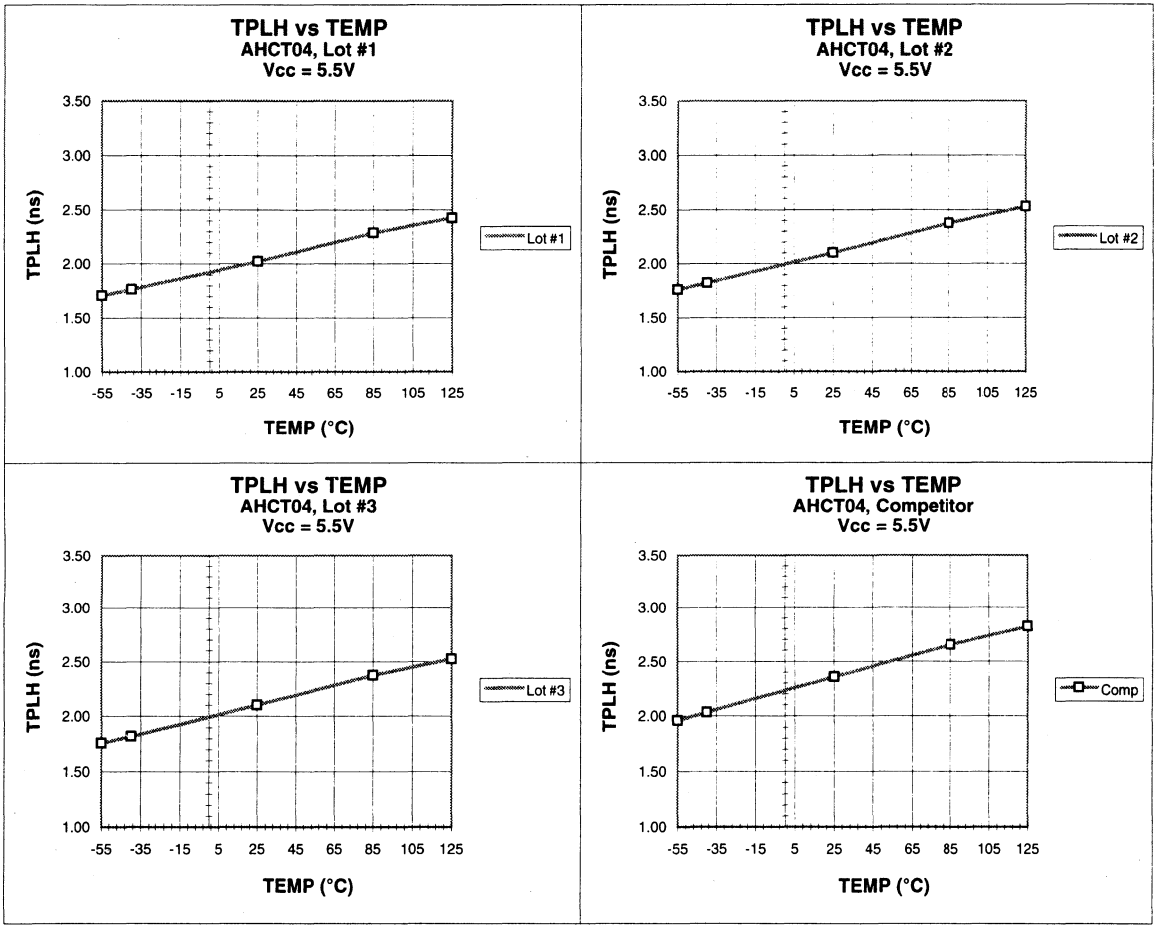

VOL vs IOL
AHCT04, Pin 2, Lot #1
Vcc = 4.5V
VOL (V)
3.00
2.50
2.00
1.50
1.00
0.50
0.00
0
10
20
30
40
50
60
IOL (mA)
25°C
VOL vs IOL
AHCT04, Pin 2, Lot #2
Vcc = 4.5V
VOL (V)
IOL (mA)
25°C
VOL vs IOL
AHCT04, Pin 2, Lot #3
Vcc = 4.5V
VOL (V)
IOL (mA)
25°C
VOL vs IOL
AHCT04, Pin 2, Competitor
Vcc = 4.5V
VOL (V)
IOL (mA)
25°C

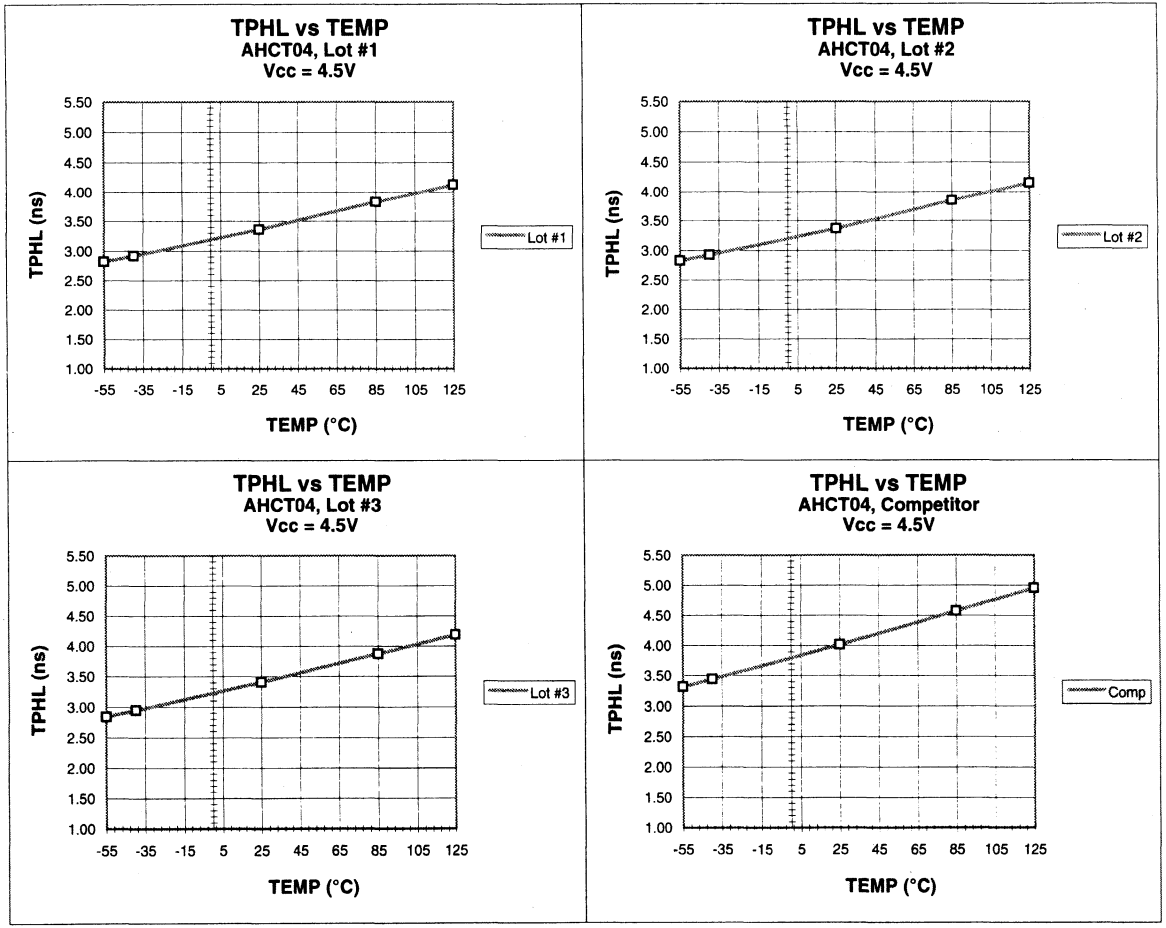

VOL vs IOL
AHCT04, Pin 2, Lot #1
Vcc = 5.5V
VOL (V)
3.00
2.50
2.00
1.50
1.00
0.50
0.00
-10
10
30
50
70
IOL (mA)
25°C
VOL vs IOL
AHCT04, Pin 2, Lot #2
Vcc = 5.5V
VOL (V)
IOL (mA)
25°C
VOL vs iOL
AHCT04, Pin 2, Lot #3
Vcc = 5.5V
VOL (V)
IOL (mA)
25°C
VOL vs IOL
AHCT04, Pin 2, Competitor
Vcc = 5.5V
VOL (V)
IOL (mA)
25°C

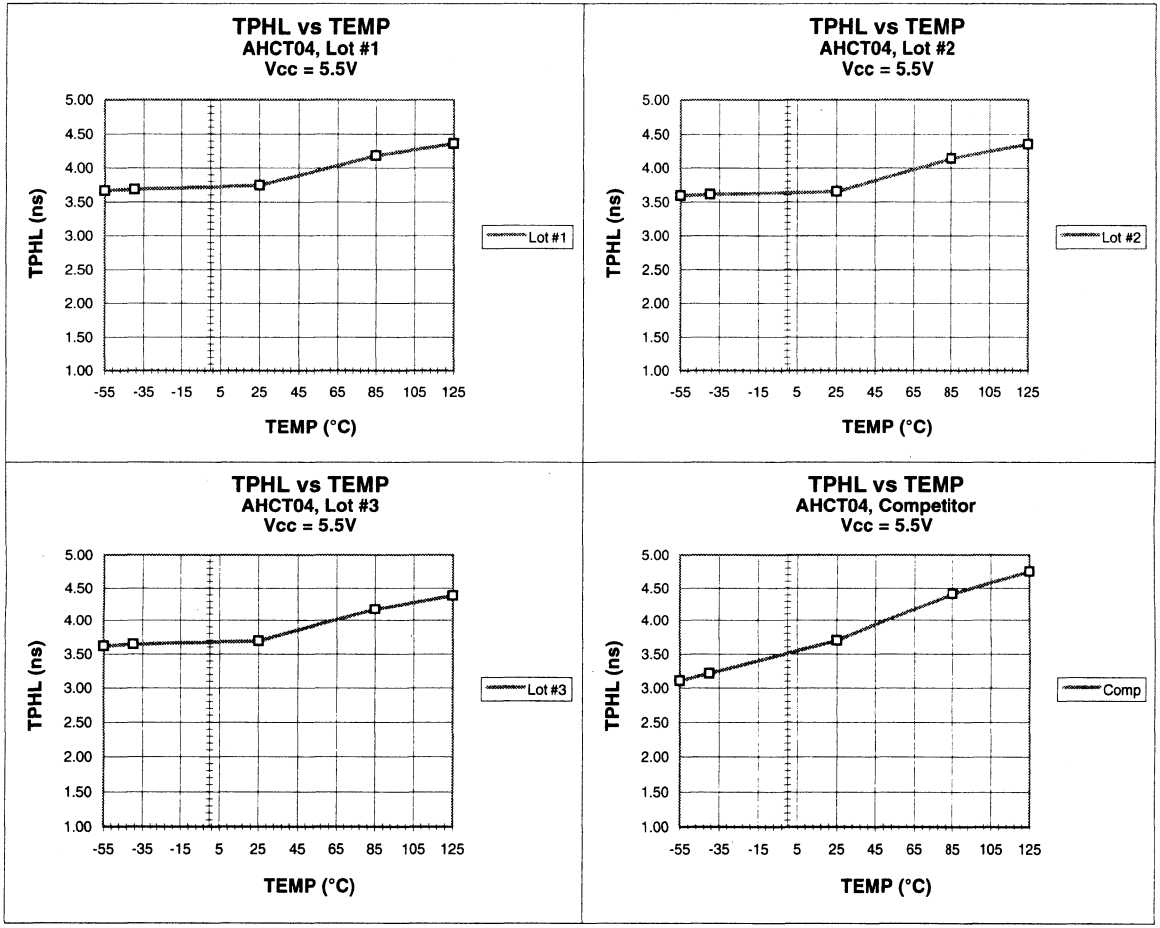

VOH vs IOH
AHCT04, Pin 2, Lot #1
Vcc = 4.5V
VOH (V)
5.00
4.50
4.00
3.50
3.00
2.50
2.00
1.50
1.00
0.50
0.00
0
-10
-20
-30
-40
-50
-60
IOH (mA)
25°C
VOH vs IOH
AHCT04, Pin 2, Lot #2
Vcc = 4.5V
VOH (V)
5.00
4.50
4.00
3.50
3.00
2.50
2.00
1.50
1.00
0.50
0.00
0
-10
-20
-30
-40
-50
-60
IOH (mA)
25°C
VOH vs IOH
AHCT04, Pin 2, Lot #3
Vcc = 4.5V
VOH (V)
5.00
4.50
4.00
3.50
3.00
2.50
2.00
1.50
1.00
0.50
0.00
0
-10
-20
-30
-40
-50
-60
IOH (mA)
25°C
VOH vs IOH
AHCT04, Pin 2, Competitor
Vcc = 4.5V
VOH (V)
5.00
4.50
4.00
3.50
3.00
2.50
2.00
1.50
1.00
0.50
0.00
0
-50
-100
-150
-200
IOH (mA)
25°C


VOH vs IOH
AHCT04, Pin 2, Lot #1
Vcc = 5.5V
VOH (V)
IOH (mA)
25°C
VOH vs IOH
AHCT04, Pin 2, Lot #2
Vcc = 5.5V
VOH (V)
IOH (mA)
25°C
VOH vs IOH
AHCT04, Pin 2, Lot #3
Vcc = 5.5V
VOH (V)
IOH (mA)
25°C
VOH vs IOH
AHCT04, Pin 2, Competitor
Vcc = 5.5V
VOH (V)
IOH (mA)
25°C


TPLH vs TEMP
AHCT04, Lot #1
Vcc = 4.5V
TPLH (ns)
4.00
3.50
3.00
2.50
2.00
1.50
1.00
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Lot #1
TPLH vs TEMP
AHCT04, Lot #2
Vcc = 4.5V
TPLH (ns)
4.00
3.50
3.00
2.50
2.00
1.50
1.00
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Lot #2
TPLH vs TEMP
AHCT04, Lot #3
Vcc = 4.5V
TPLH (ns)
4.00
3.50
3.00
2.50
2.00
1.50
1.00
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Lot #3
TPLH vs TEMP
AHCT04, Competitor
Vcc = 4.5V
TPLH (ns)
4.00
3.50
3.00
2.50
2.00
1.50
1.00
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Comp

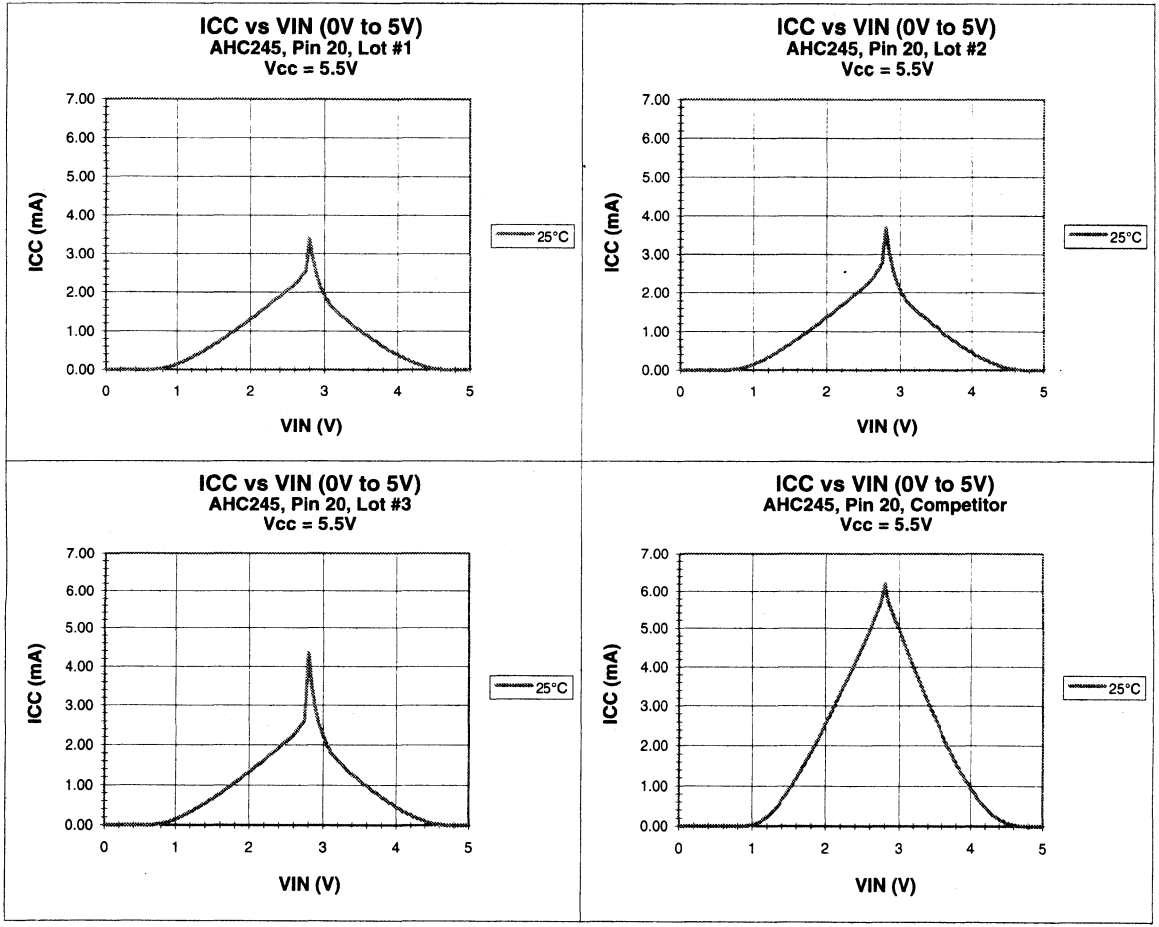

TPLH vs TEMP
AHCT04, Lot #1
Vcc = 5.5V
TPLH (ns)
3.50
3.00
2.50
2.00
1.50
1.00
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Lot #1
TPLH vs TEMP
AHCT04, Lot #2
Vcc = 5.5V
TPLH (ns)
3.50
3.00
2.50
2.00
1.50
1.00
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Lot #2
TPLH vs TEMP
AHCT04, Lot #3
Vcc = 5.5V
TPLH (ns)
3.50
3.00
2.50
2.00
1.50
1.00
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Lot #3
TPLH vs TEMP
AHCT04, Competitor
Vcc = 5.5V
TPLH (ns)
3.50
3.00
2.50
2.00
1.50
1.00
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Comp

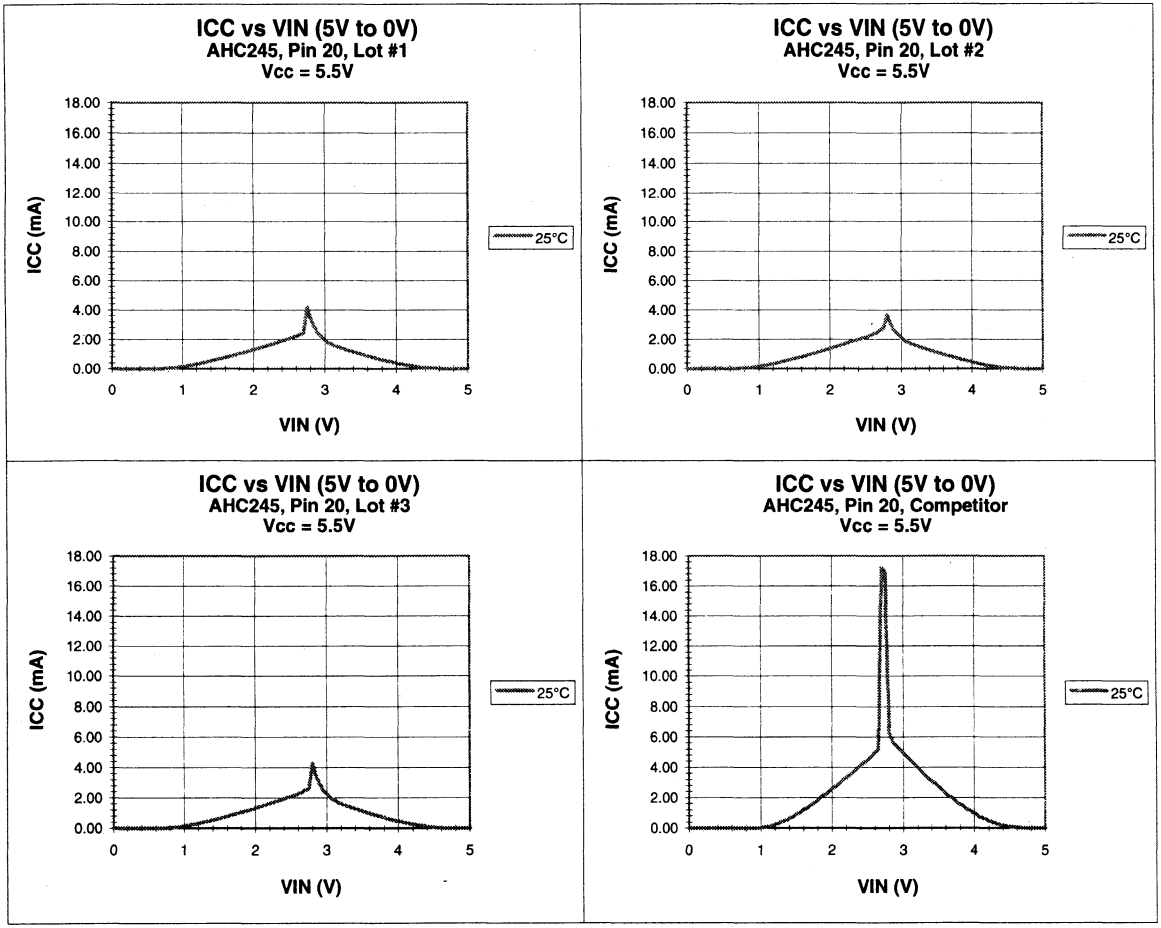

TPHL vs TEMP
AHCT04, Lot #1
Vcc = 4.5V
TPHL (ns)
5.50
5.00
4.50
4.00
3.50
3.00
2.50
2.00
1.50
1.00
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Lot #1
TPHL vs TEMP
AHCT04, Lot #2
Vcc = 4.5V
TPHL (ns)
5.50
5.00
4.50
4.00
3.50
3.00
2.50
2.00
1.50
1.00
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Lot #2
TPHL vs TEMP
AHCT04, Lot #3
Vcc = 4.5V
TPHL (ns)
5.50
5.00
4.50
4.00
3.50
3.00
2.50
2.00
1.50
1.00
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Lot #3
TPHL vs TEMP
AHCT04, Competitor
Vcc = 4.5V
TPHL (ns)
5.50
5.00
4.50
4.00
3.50
3.00
2.50
2.00
1.50
1.00
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Comp

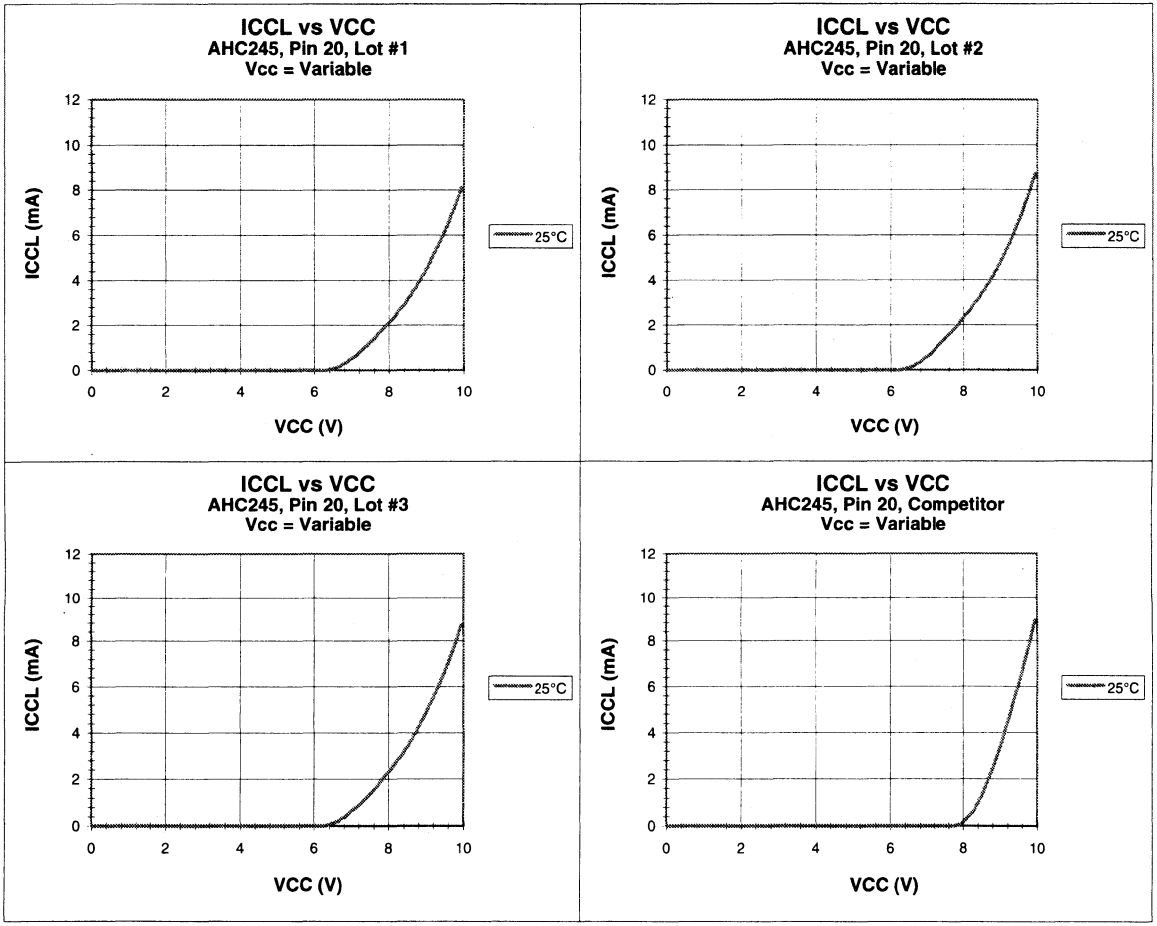

TPHL vs TEMP
AHCT04, Lot #1
Vcc = 5.5V
TPHL (ns)
5.00
4.50
4.00
3.50
3.00
2.50
2.00
1.50
1.00
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Lot #1
TPHL vs TEMP
AHCT04, Lot #2
Vcc = 5.5V
TPHL (ns)
5.00
4.50
4.00
3.50
3.00
2.50
2.00
1.50
1.00
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Lot #2
TPHL vs TEMP
AHCT04, Lot #3
Vcc = 5.5V
TPHL (ns)
5.00
4.50
4.00
3.50
3.00
2.50
2.00
1.50
1.00
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Lot #3
TPHL vs TEMP
AHCT04, Competitor
Vcc = 5.5V
TPHL (ns)
5.00
4.50
4.00
3.50
3.00
2.50
2.00
1.50
1.00
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Comp

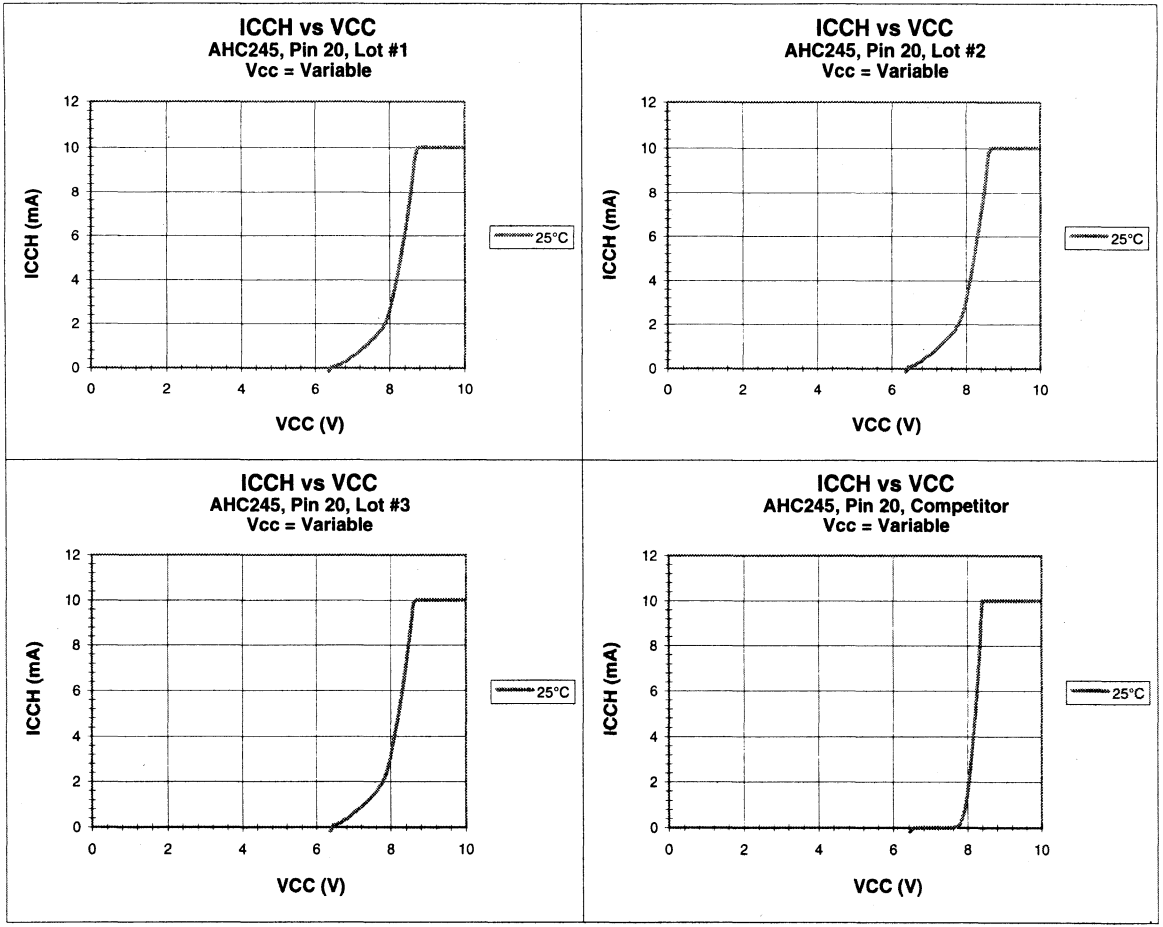
General Information 1
AHC Data Sheets 2
AHCT Data Sheets 3
Mechanical Data 4
AHC04 Qualification Data A
AHCT04 Qualification Data B
AHC245 Qualification Data C
AHCT245 Qualification Data D

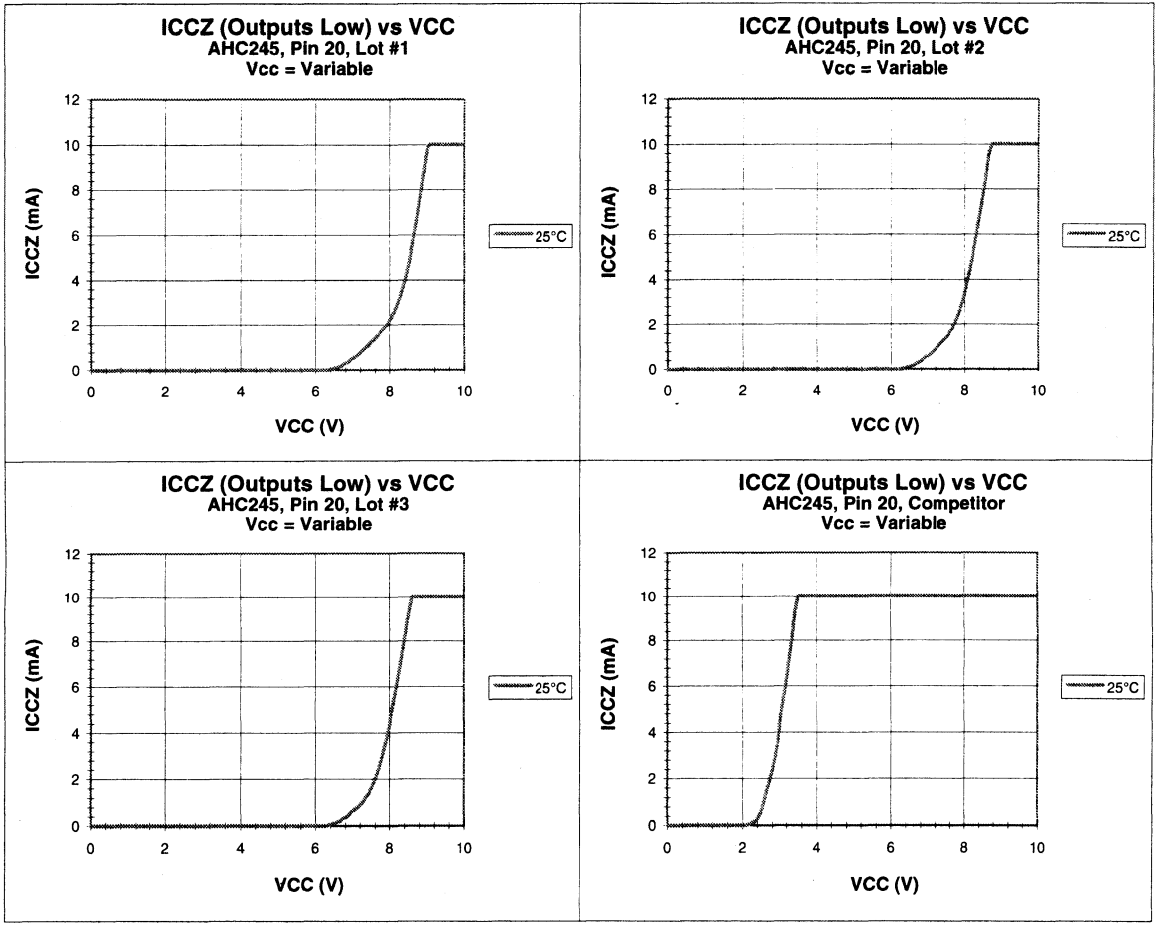
AHC245 Qualification Data

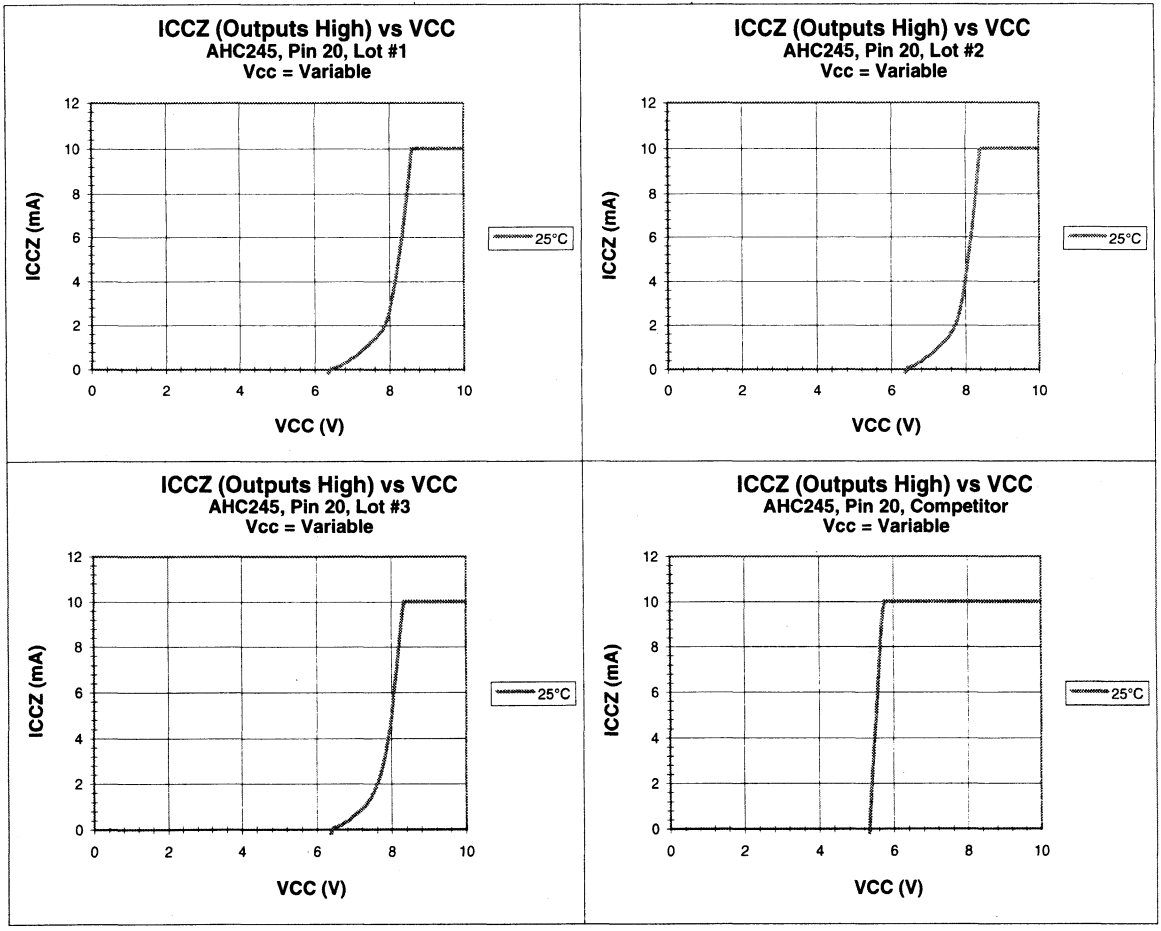

ICC vs VIN (0V to 5V)
AHC245, Pin 20, Lot #1
Vcc = 5.5V
ICC (mA)
7.00
6.00
5.00
4.00
3.00
2.00
1.00
0.00
0
1
2
3
4
5
VIN (V)
25°C
ICC vs VIN (0V to 5V)
AHC245, Pin 20, Lot #2
Vcc = 5.5V
ICC (mA)
VIN (V)
25°C
ICC vs VIN (0V to 5V)
AHC245, Pin 20, Lot #3
Vcc = 5.5V
ICC (mA)
VIN (V)
25°C
ICC vs VIN (0V to 5V)
AHC245, Pin 20, Competitor
Vcc = 5.5V
ICC (mA)
VIN (V)
25°C

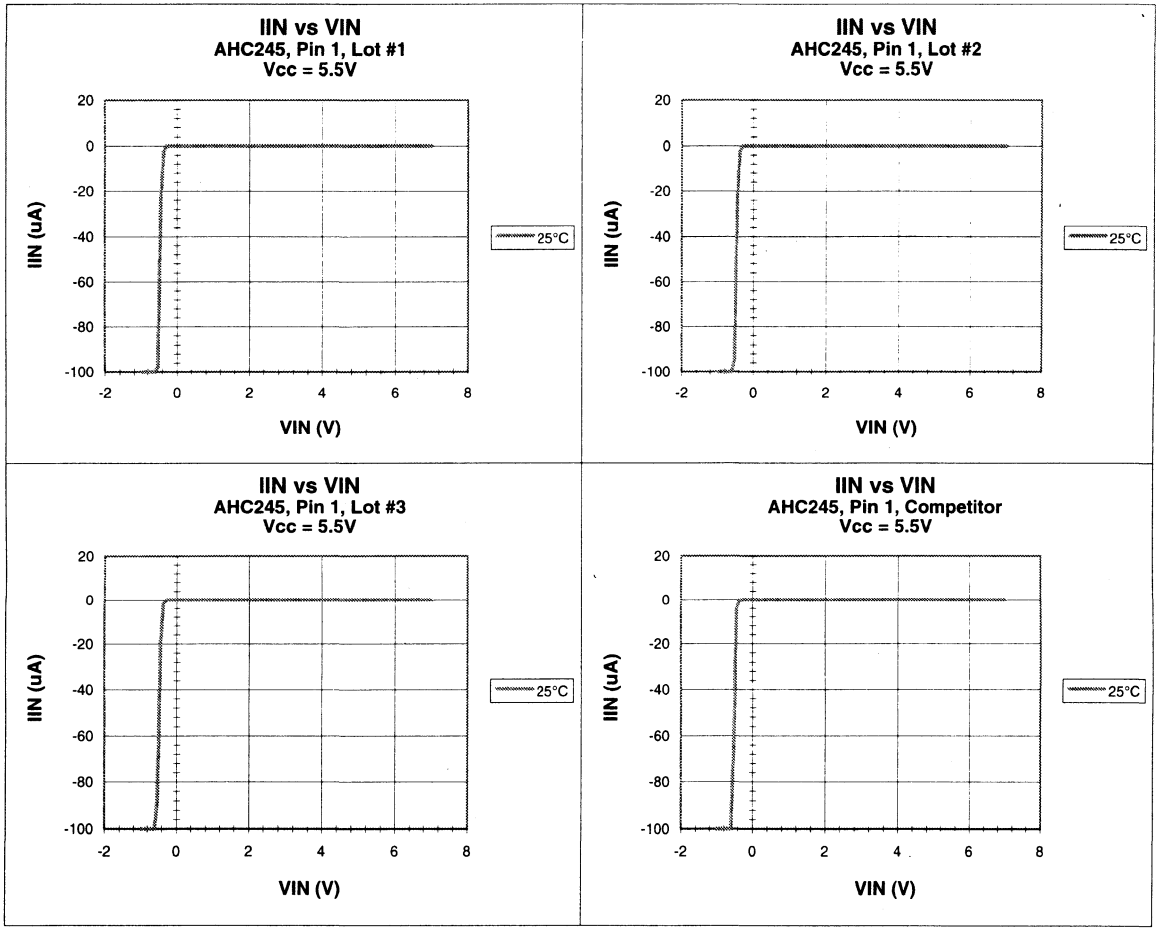

ICC vs VIN (5V to 0V)
AHC245, Pin 20, Lot #1
Vcc = 5.5V
ICC (mA)
18.00
16.00
14.00
12.00
10.00
8.00
6.00
4.00
2.00
0.00
0
1
2
3
4
5
VIN (V)
25°C
ICC vs VIN (5V to 0V)
AHC245, Pin 20, Lot #2
Vcc = 5.5V
ICC (mA)
VIN (V)
25°C
ICC vs VIN (5V to 0V)
AHC245, Pin 20, Lot #3
Vcc = 5.5V
ICC (mA)
VIN (V)
25°C
ICC vs VIN (5V to 0V)
AHC245, Pin 20, Competitor
Vcc = 5.5V
ICC (mA)
VIN (V)
25°C

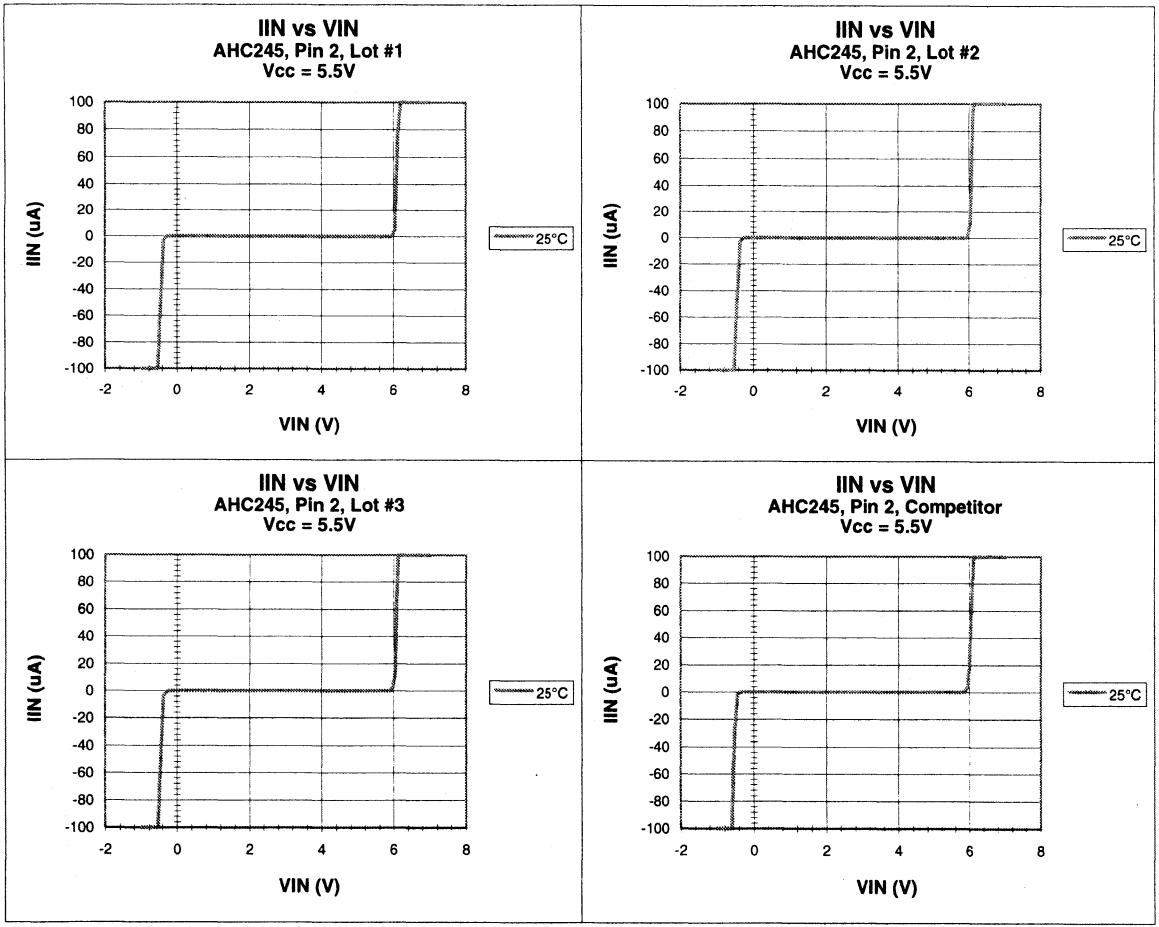

ICCL vs VCC
AHC245, Pin 20, Lot #1
Vcc = Variable
ICCL (mA)
VCC (V)
25°C
ICCL vs VCC
AHC245, Pin 20, Lot #2
Vcc = Variable
ICCL (mA)
VCC (V)
25°C
ICCL vs VCC
AHC245, Pin 20, Lot #3
Vcc = Variable
ICCL (mA)
VCC (V)
25°C
ICCL vs VCC
AHC245, Pin 20, Competitor
Vcc = Variable
ICCL (mA)
VCC (V)
25°C

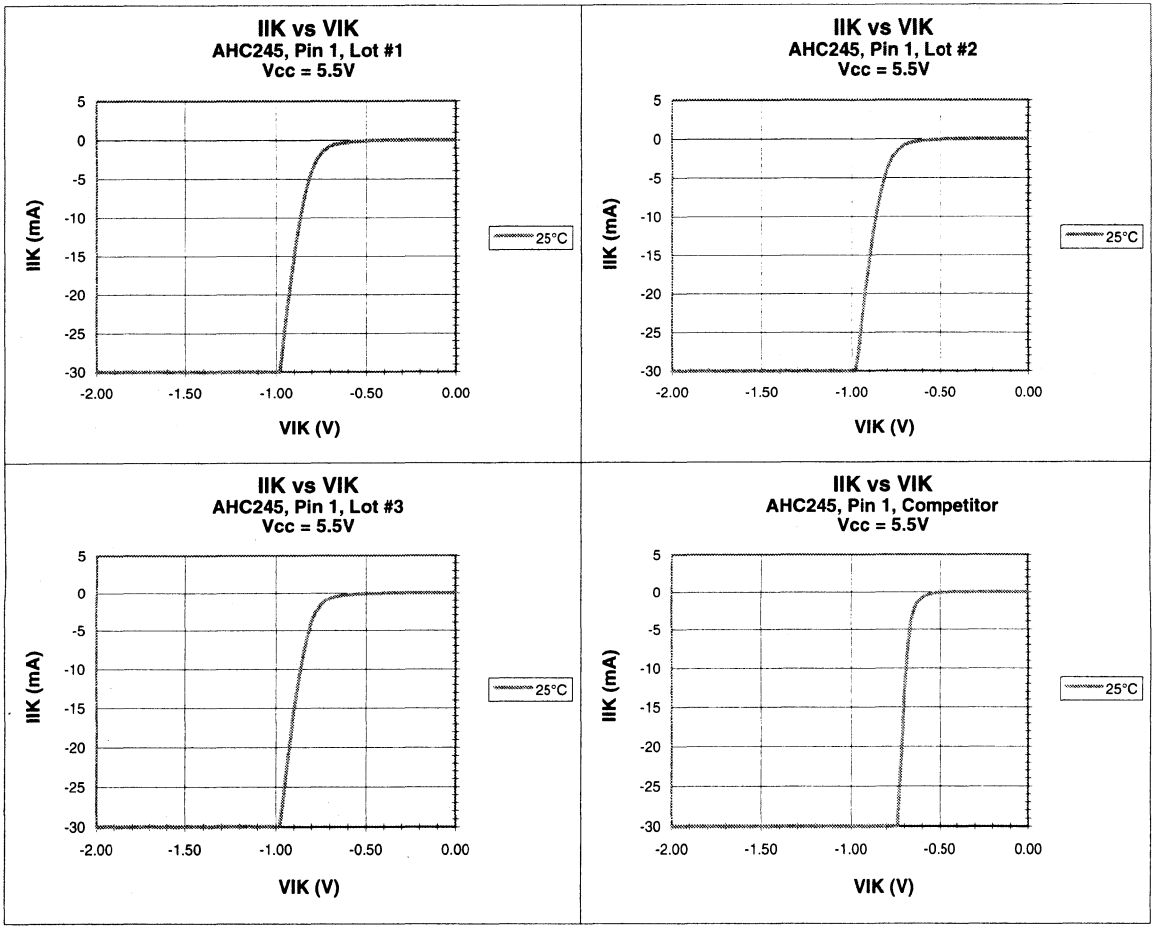

ICCH vs VCC
AHC245, Pin 20, Lot #1
Vcc = Variable
ICCH (mA)
VCC (V)
25°C
ICCH vs VCC
AHC245, Pin 20, Lot #2
Vcc = Variable
ICCH (mA)
VCC (V)
25°C
ICCH vs VCC
AHC245, Pin 20, Lot #3
Vcc = Variable
ICCH (mA)
VCC (V)
25°C
ICCH vs VCC
AHC245, Pin 20, Competitor
Vcc = Variable
ICCH (mA)
VCC (V)
25°C

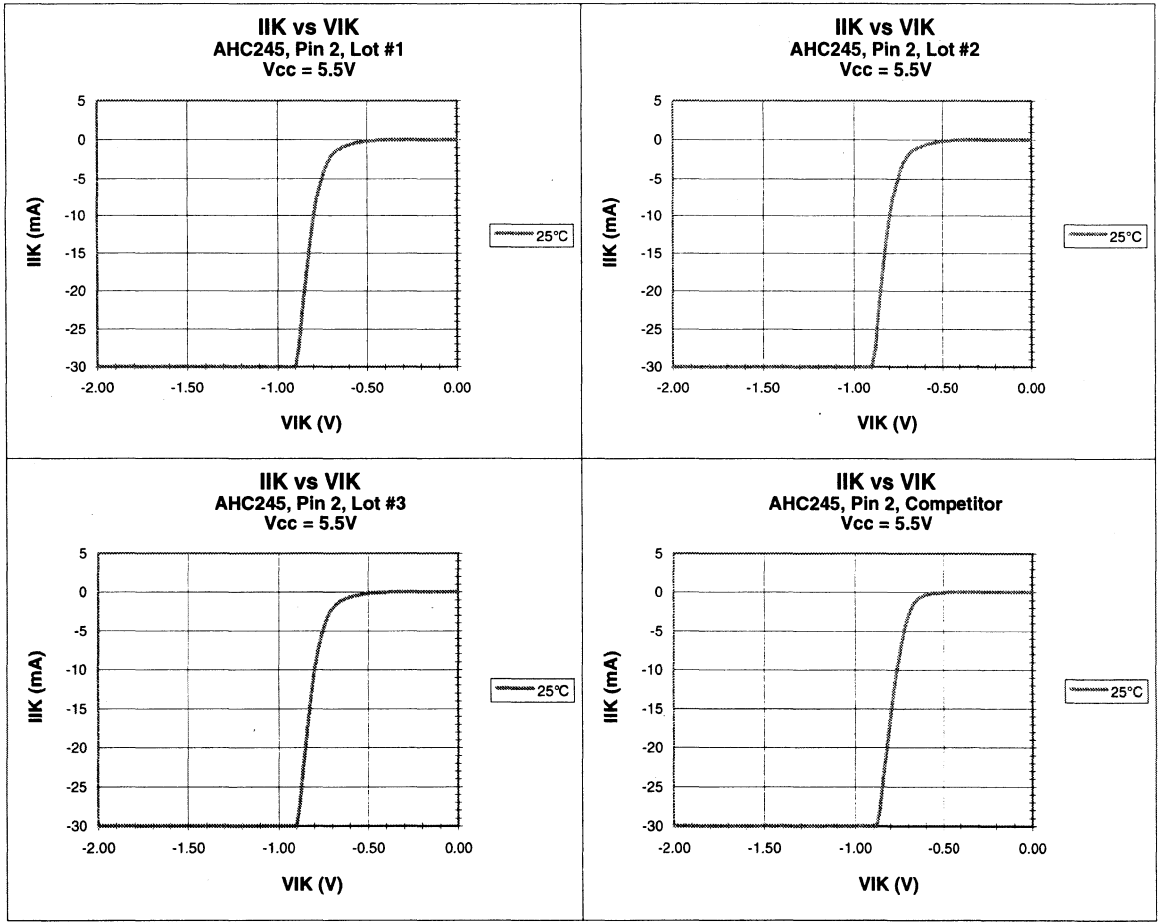

ICCZ (Outputs Low) vs VCC
AHC245, Pin 20, Lot #1
Vcc = Variable
ICCZ (mA)
VCC (V)
25°C
ICCZ (Outputs Low) vs VCC
AHC245, Pin 20, Lot #2
Vcc = Variable
ICCZ (mA)
VCC (V)
25°C
ICCZ (Outputs Low) vs VCC
AHC245, Pin 20, Lot #3
Vcc = Variable
ICCZ (mA)
VCC (V)
25°C
ICCZ (Outputs Low) vs VCC
AHC245, Pin 20, Competitor
Vcc = Variable
ICCZ (mA)
VCC (V)
25°C

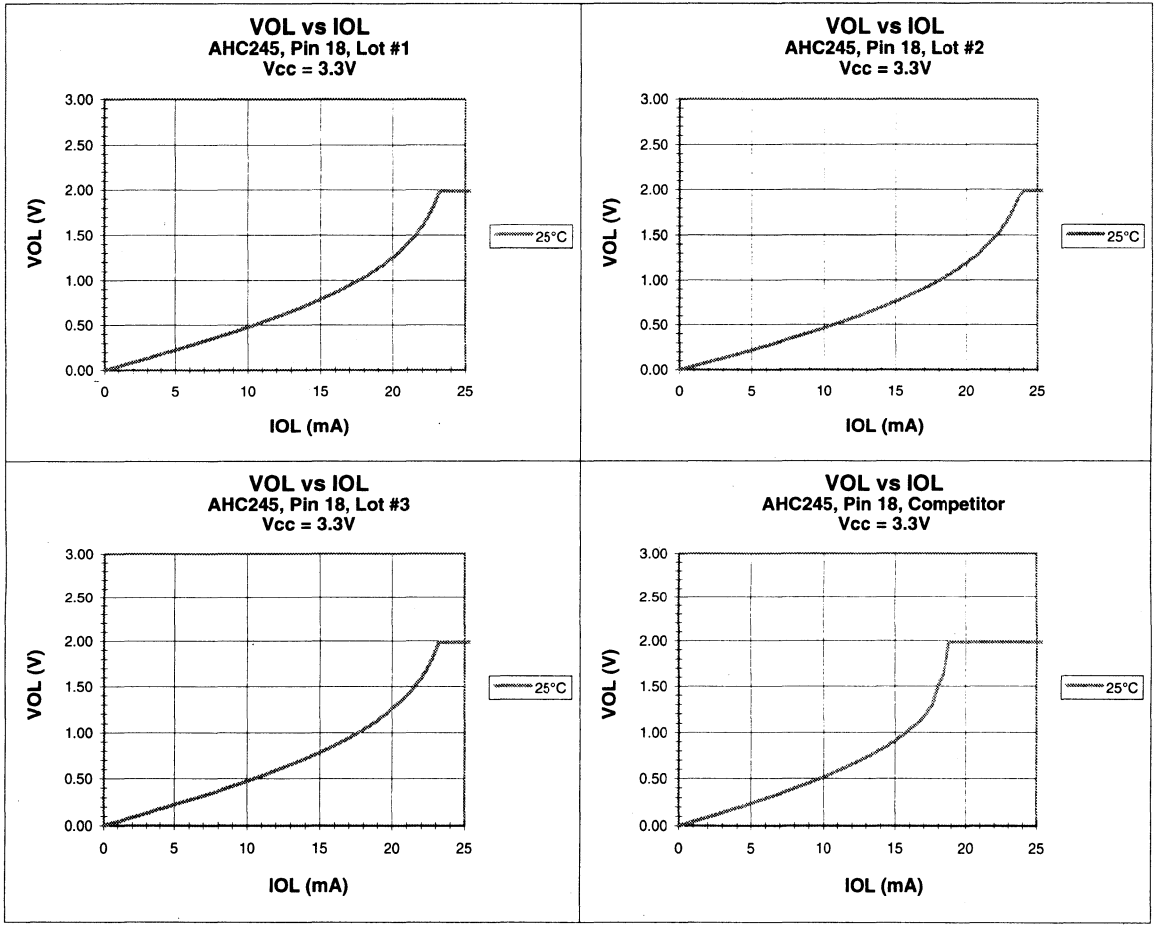

ICCZ (Outputs High) vs VCC
AHC245, Pin 20, Lot #1
Vcc = Variable
ICCZ (mA)
VCC (V)
25°C
ICCZ (Outputs High) vs VCC
AHC245, Pin 20, Lot #2
Vcc = Variable
ICCZ (mA)
VCC (V)
25°C
ICCZ (Outputs High) vs VCC
AHC245, Pin 20, Lot #3
Vcc = Variable
ICCZ (mA)
VCC (V)
25°C
ICCZ (Outputs High) vs VCC
AHC245, Pin 20, Competitor
Vcc = Variable
ICCZ (mA)
VCC (V)
25°C

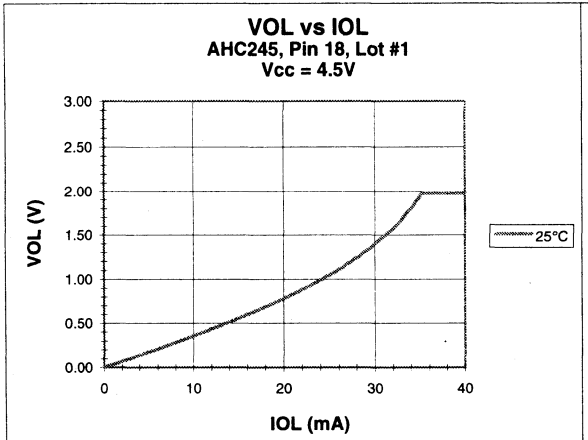

IIN vs VIN
AHC245, Pin 1, Lot #1
Vcc = 5.5V
IIN (uA)
VIN (V)
25°C
IIN vs VIN
AHC245, Pin 1, Lot #2
Vcc = 5.5V
IIN (uA)
VIN (V)
25°C
IIN vs VIN
AHC245, Pin 1, Lot #3
Vcc = 5.5V
IIN (uA)
VIN (V)
25°C
IIN vs VIN
AHC245, Pin 1, Competitor
Vcc = 5.5V
IIN (uA)
VIN (V)
25°C

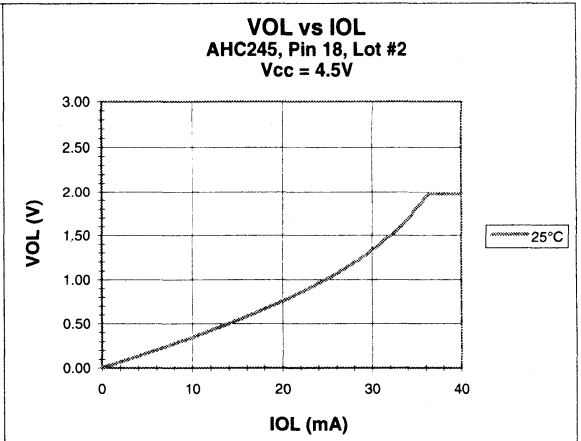

IIN vs VIN
AHC245, Pin 2, Lot #1
Vcc = 5.5V
IIN (uA)
VIN (V)
25°C
IIN vs VIN
AHC245, Pin 2, Lot #2
Vcc = 5.5V
IIN (uA)
VIN (V)
25°C
IIN vs VIN
AHC245, Pin 2, Lot #3
Vcc = 5.5V
IIN (uA)
VIN (V)
25°C
IIN vs VIN
AHC245, Pin 2, Competitor
Vcc = 5.5V
IIN (uA)
VIN (V)
25°C

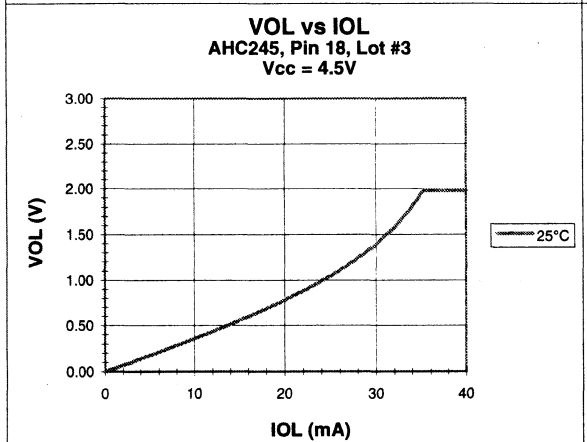

IIK vs VIK
AHC245, Pin 1, Lot #1
Vcc = 5.5V
IIK (mA)
5
0
-5
-10
-15
-20
-25
-30
-2.00
-1.50
-1.00
-0.50
0.00
VIK (V)
25°C
IIK vs VIK
AHC245, Pin 1, Lot #2
Vcc = 5.5V
IIK (mA)
VIK (V)
25°C
IIK vs VIK
AHC245, Pin 1, Lot #3
Vcc = 5.5V
IIK (mA)
VIK (V)
25°C
IIK vs VIK
AHC245, Pin 1, Competitor
Vcc = 5.5V
IIK (mA)
VIK (V)
25°C

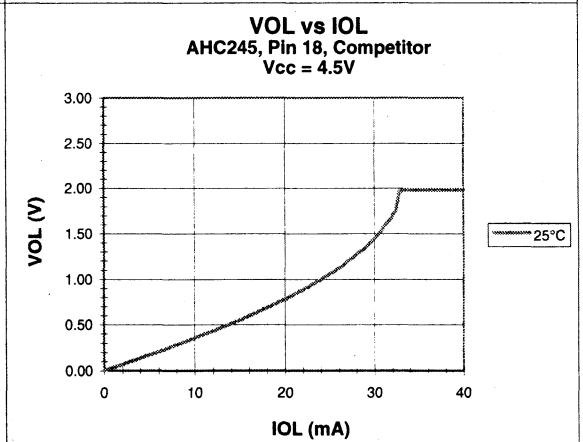

IIK vs VIK
AHC245, Pin 2, Lot #1
Vcc = 5.5V
IIK (mA)
5
0
-5
-10
-15
-20
-25
-30
-2.00
-1.50
-1.00
-0.50
0.00
VIK (V)
25°C
IIK vs VIK
AHC245, Pin 2, Lot #2
Vcc = 5.5V
IIK (mA)
VIK (V)
25°C
IIK vs VIK
AHC245, Pin 2, Lot #3
Vcc = 5.5V
IIK (mA)
VIK (V)
25°C
IIK vs VIK
AHC245, Pin 2, Competitor
Vcc = 5.5V
IIK (mA)
VIK (V)
25°C

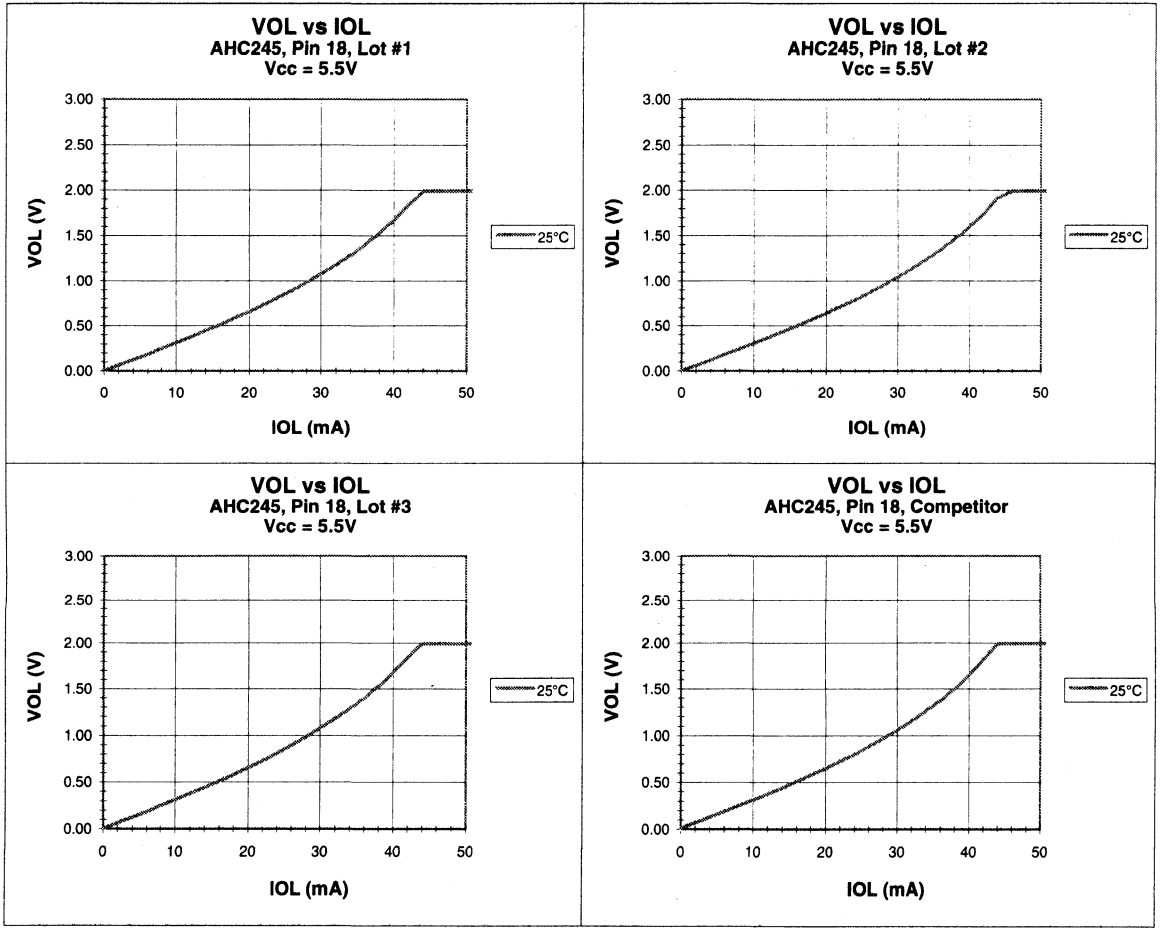

VOL vs IOL
AHC245, Pin 18, Lot #1
Vcc = 3.3V
VOL (V)
3.00
2.50
2.00
1.50
1.00
0.50
0.00
0
5
10
15
20
25
IOL (mA)
25°C
VOL vs IOL
AHC245, Pin 18, Lot #2
Vcc = 3.3V
VOL (V)
IOL (mA)
25°C
VOL vs IOL
AHC245, Pin 18, Lot #3
Vcc = 3.3V
VOL (V)
IOL (mA)
25°C
VOL vs IOL
AHC245, Pin 18, Competitor
Vcc = 3.3V
VOL (V)
IOL (mA)
25°C

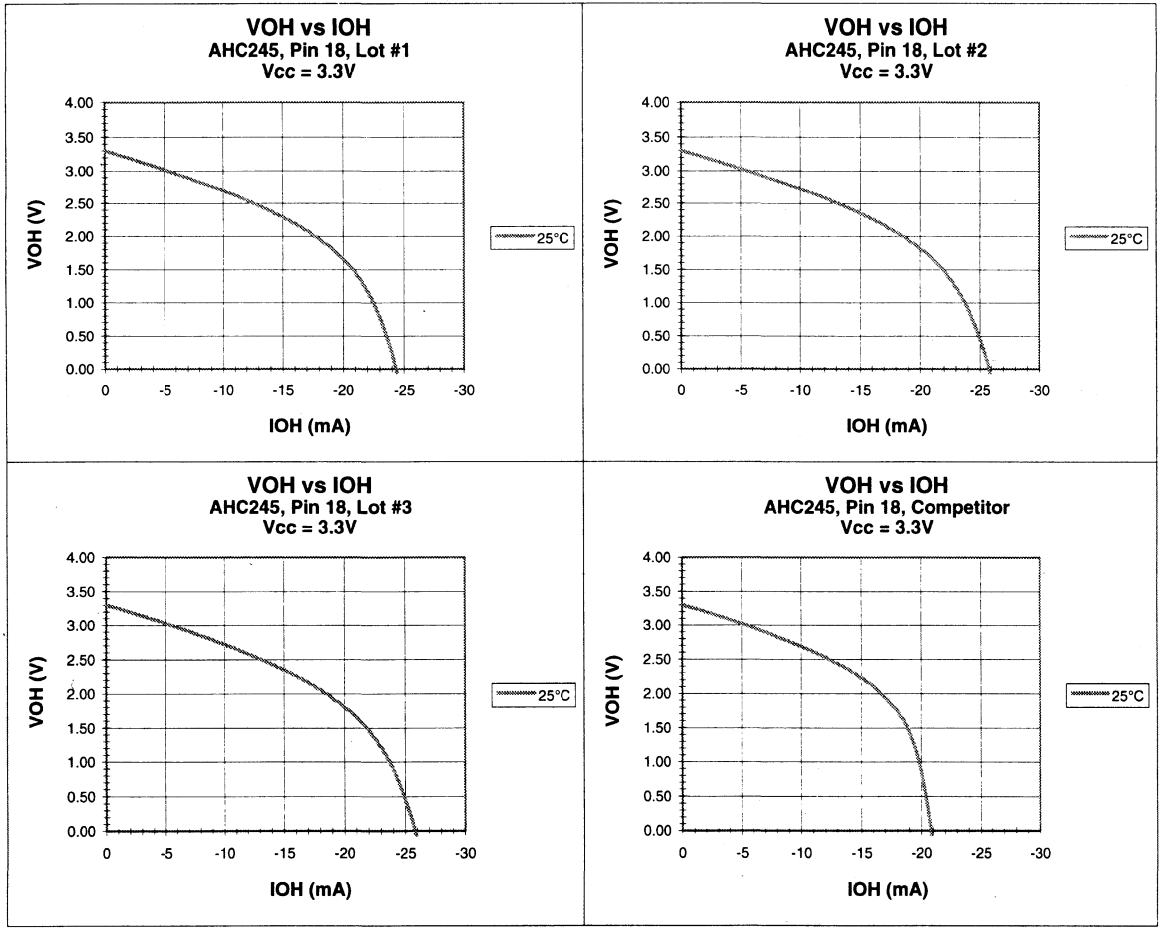

VOL vs IOL
AHC245, Pin 18, Lot #1
Vcc = 4.5V
VOL (V)
3.00
2.50
2.00
1.50
1.00
0.50
0.00
0
10
20
30
40
IOL (mA)
25°C

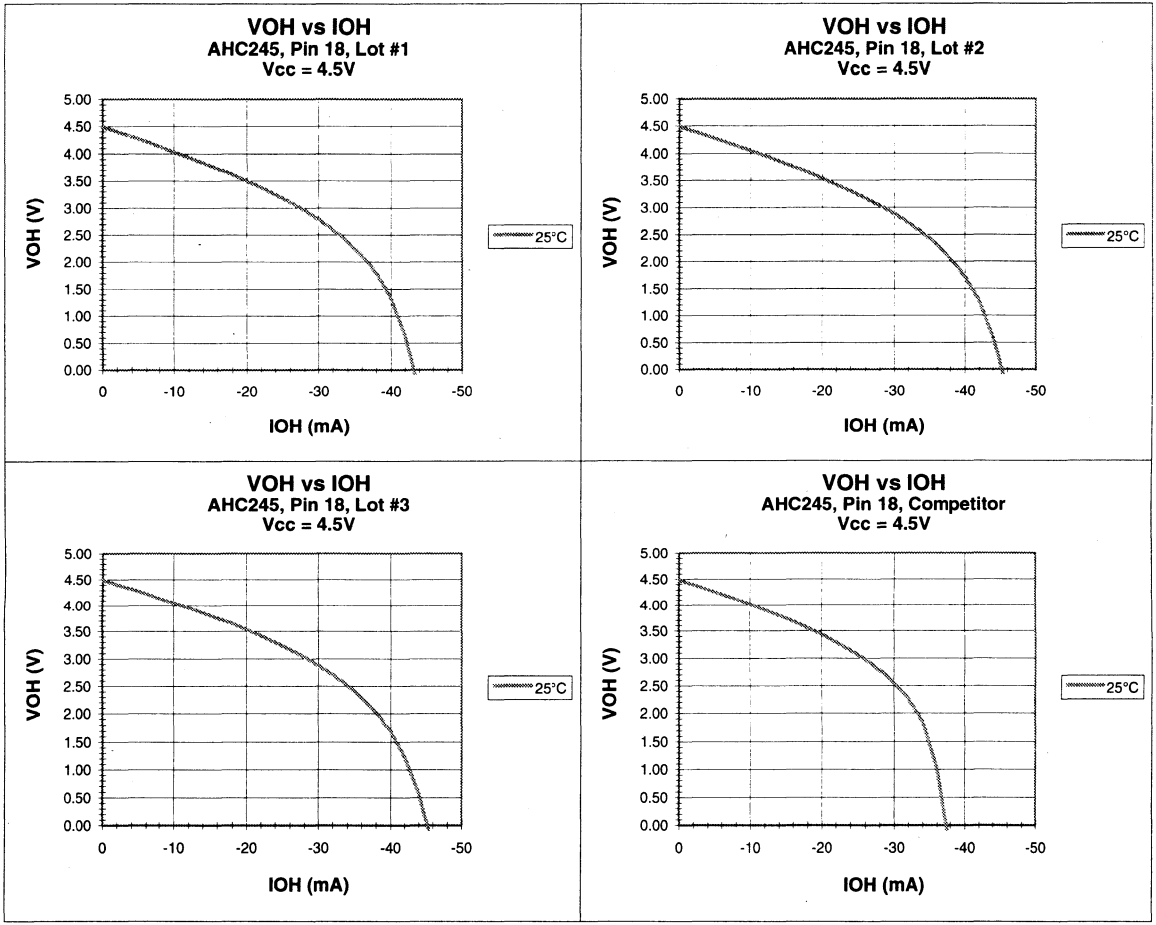

VOL vs IOL
AHC245, Pin 18, Lot #2
Vcc = 4.5V
VOL (V)
3.00
2.50
2.00
1.50
1.00
0.50
0.00
0
10
20
30
40
IOL (mA)
25°C

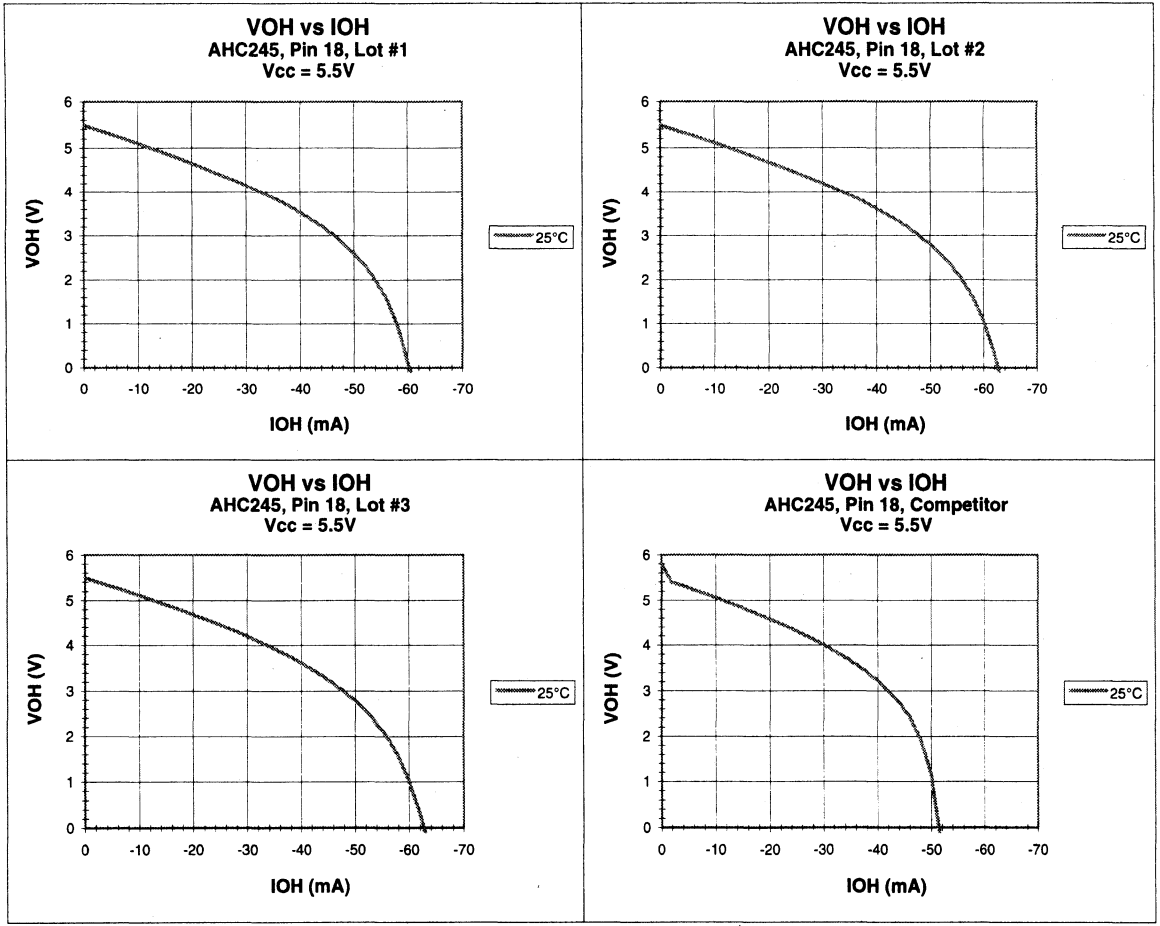

VOL vs IOL
AHC245, Pin 18, Lot #3
Vcc = 4.5V
VOL (V)
3.00
2.50
2.00
1.50
1.00
0.50
0.00
0
10
20
30
40
IOL (mA)
25°C

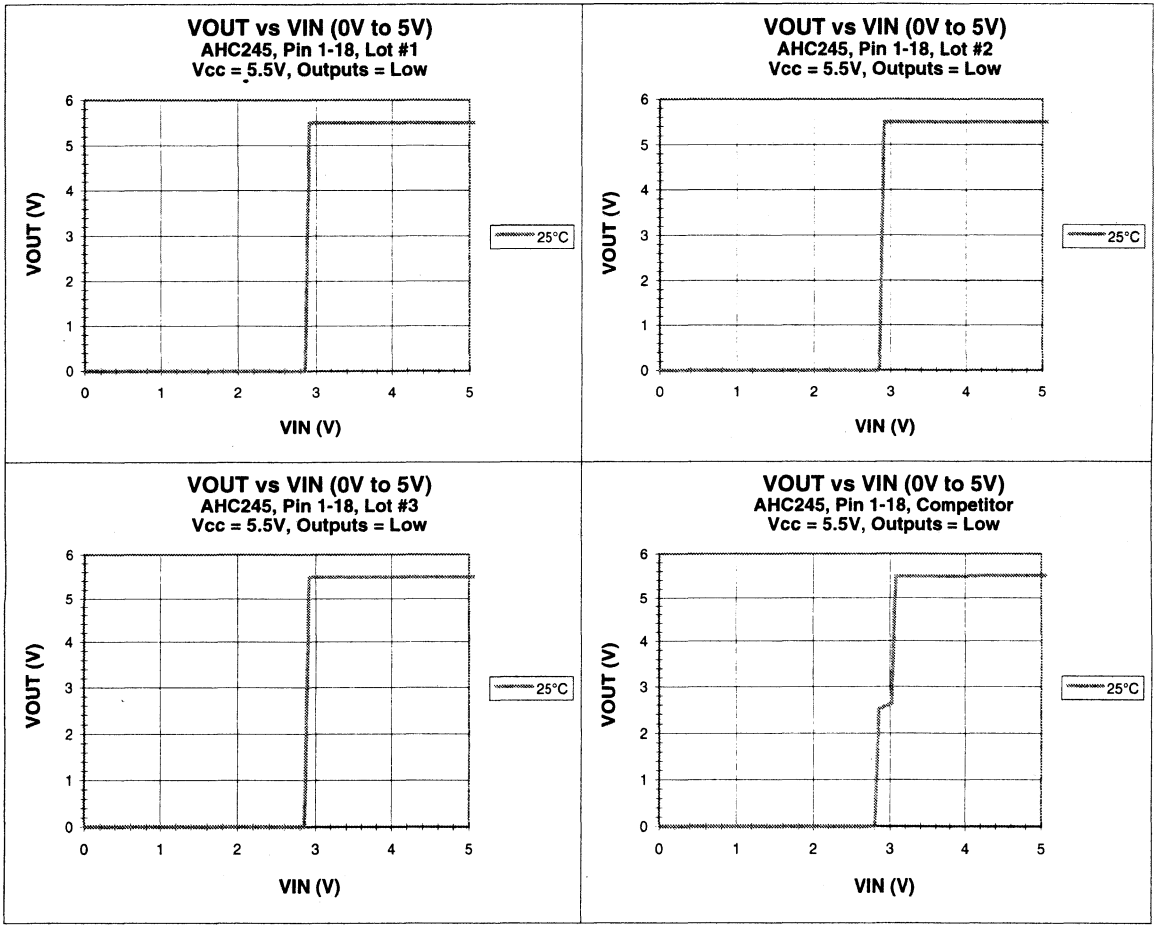

VOL vs IOL
AHC245, Pin 18, Competitor
Vcc = 4.5V
VOL (V)
3.00
2.50
2.00
1.50
1.00
0.50
0.00
0
10
20
30
40
IOL (mA)
25°C

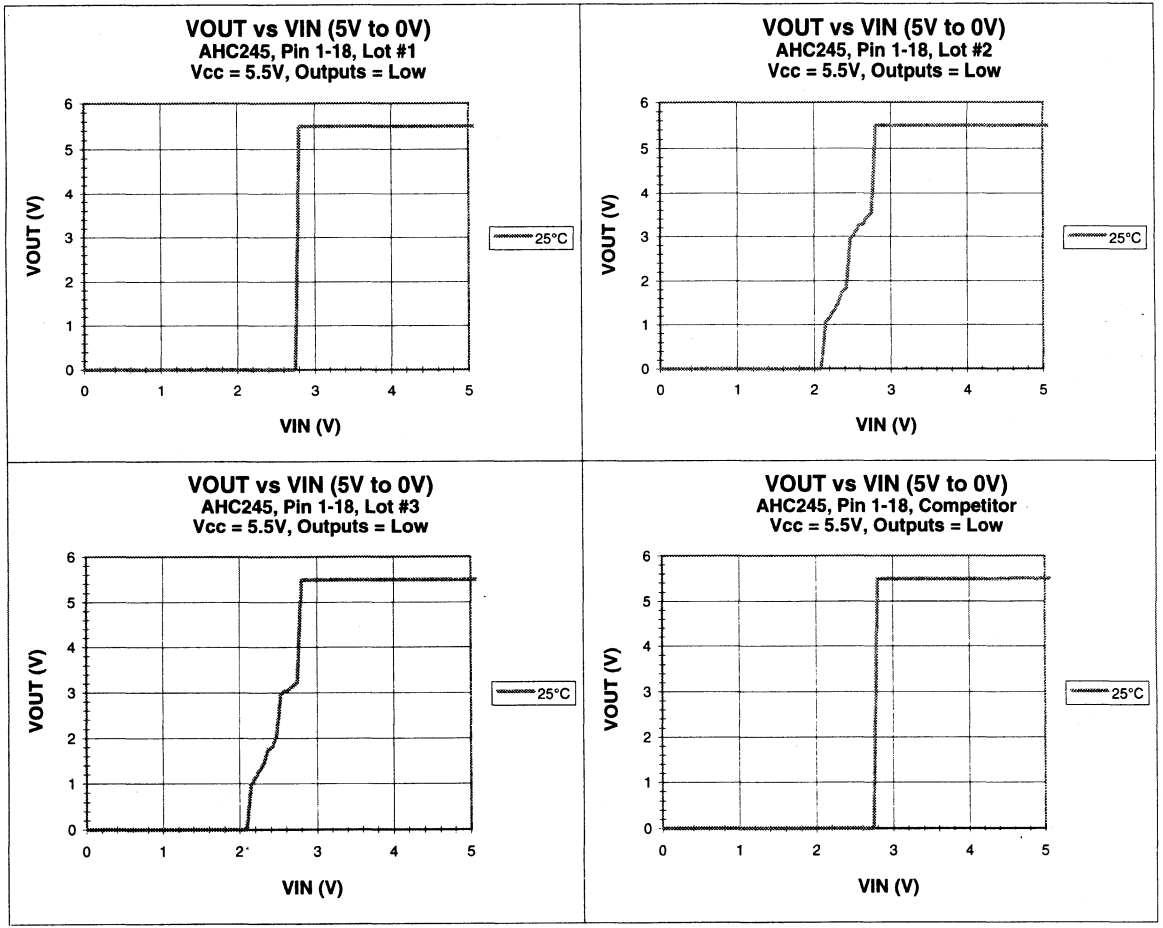

VOL vs IOL
AHC245, Pin 18, Lot #1
Vcc = 5.5V
VOL (V)
3.00
2.50
2.00
1.50
1.00
0.50
0.00
0
10
20
30
40
50
IOL (mA)
25°C
VOL vs IOL
AHC245, Pin 18, Lot #2
Vcc = 5.5V
VOL (V)
IOL (mA)
25°C
VOL vs IOL
AHC245, Pin 18, Lot #3
Vcc = 5.5V
VOL (V)
IOL (mA)
25°C
VOL vs IOL
AHC245, Pin 18, Competitor
Vcc = 5.5V
VOL (V)
IOL (mA)
25°C

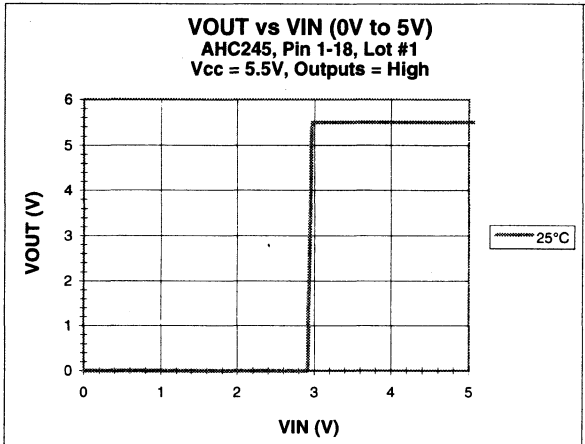

VOH vs IOH
AHC245, Pin 18, Lot #1
Vcc = 3.3V
VOH (V)
4.00
3.50
3.00
2.50
2.00
1.50
1.00
0.50
0.00
0
-5
-10
-15
-20
-25
-30
IOH (mA)
25°C
VOH vs IOH
AHC245, Pin 18, Lot #2
Vcc = 3.3V
VOH (V)
IOH (mA)
25°C
VOH vs IOH
AHC245, Pin 18, Lot #3
Vcc = 3.3V
VOH (V)
IOH (mA)
25°C
VOH vs IOH
AHC245, Pin 18, Competitor
Vcc = 3.3V
VOH (V)
IOH (mA)
25°C

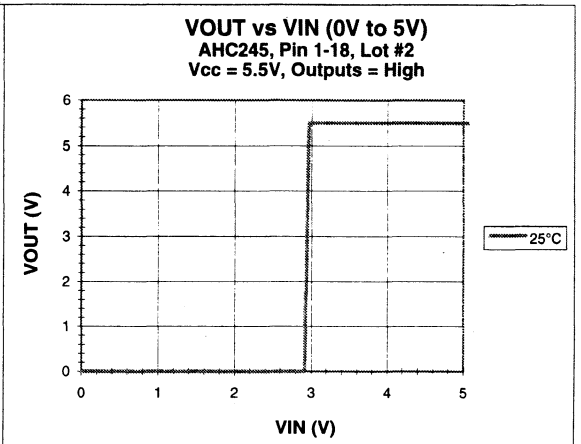

VOH vs IOH
AHC245, Pin 18, Lot #1
Vcc = 4.5V
VOH (V)
5.00
4.50
4.00
3.50
3.00
2.50
2.00
1.50
1.00
0.50
0.00
0
-10
-20
-30
-40
-50
IOH (mA)
25°C
VOH vs IOH
AHC245, Pin 18, Lot #2
Vcc = 4.5V
VOH (V)
IOH (mA)
25°C
VOH vs IOH
AHC245, Pin 18, Lot #3
Vcc = 4.5V
VOH (V)
IOH (mA)
25°C
VOH vs IOH
AHC245, Pin 18, Competitor
Vcc = 4.5V
VOH (V)
IOH (mA)
25°C

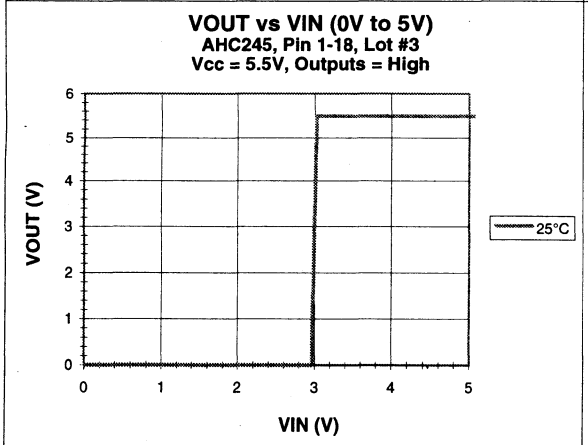

VOH vs IOH
AHC245, Pin 18, Lot #1
Vcc = 5.5V
VOH (V)
IOH (mA)
25°C
VOH vs IOH
AHC245, Pin 18, Lot #2
Vcc = 5.5V
VOH (V)
IOH (mA)
25°C
VOH vs IOH
AHC245, Pin 18, Lot #3
Vcc = 5.5V
VOH (V)
IOH (mA)
25°C
VOH vs IOH
AHC245, Pin 18, Competitor
Vcc = 5.5V
VOH (V)
IOH (mA)
25°C

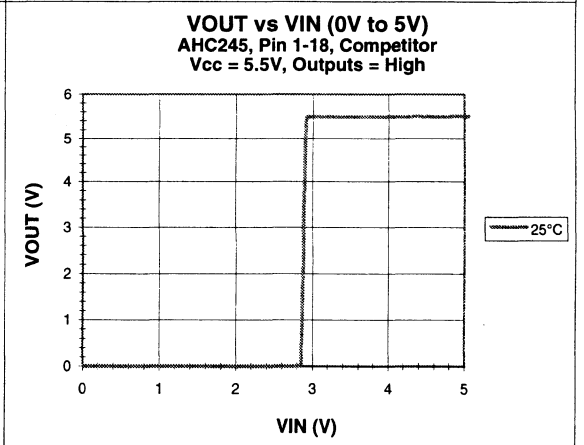

VOUT vs VIN (0V to 5V)
AHC245, Pin 1-18, Lot #1
Vcc = 5.5V, Outputs = Low
VOUT (V)
VIN (V)
25°C
VOUT vs VIN (0V to 5V)
AHC245, Pin 1-18, Lot #2
Vcc = 5.5V, Outputs = Low
VOUT (V)
VIN (V)
25°C
VOUT vs VIN (0V to 5V)
AHC245, Pin 1-18, Lot #3
Vcc = 5.5V, Outputs = Low
VOUT (V)
VIN (V)
25°C
VOUT vs VIN (0V to 5V)
AHC245, Pin 1-18, Competitor
Vcc = 5.5V, Outputs = Low
VOUT (V)
VIN (V)
25°C

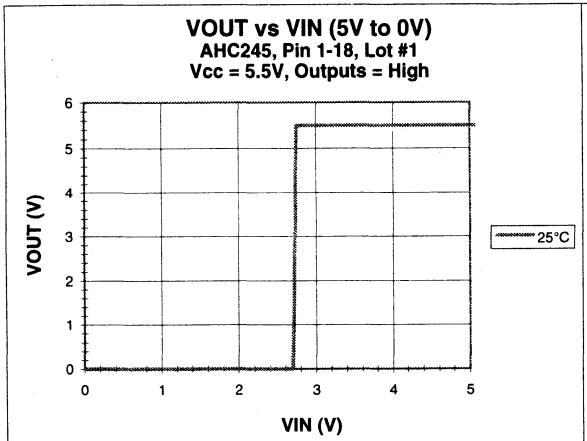

VOUT vs VIN (5V to 0V)
AHC245, Pin 1-18, Lot #1
Vcc = 5.5V, Outputs = Low
VOUT (V)
VIN (V)
25°C
VOUT vs VIN (5V to 0V)
AHC245, Pin 1-18, Lot #2
Vcc = 5.5V, Outputs = Low
VOUT (V)
VIN (V)
25°C
VOUT vs VIN (5V to 0V)
AHC245, Pin 1-18, Lot #3
Vcc = 5.5V, Outputs = Low
VOUT (V)
VIN (V)
25°C
VOUT vs VIN (5V to 0V)
AHC245, Pin 1-18, Competitor
Vcc = 5.5V, Outputs = Low
VOUT (V)
VIN (V)
25°C

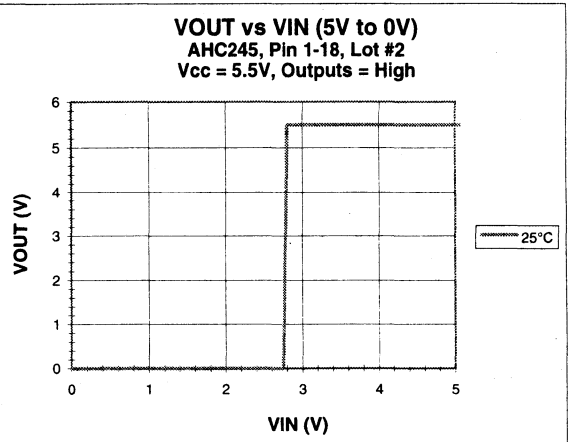

VOUT vs VIN (0V to 5V)
AHC245, Pin 1-18, Lot #1
Vcc = 5.5V, Outputs = High
VOUT (V)
VIN (V)
25°C

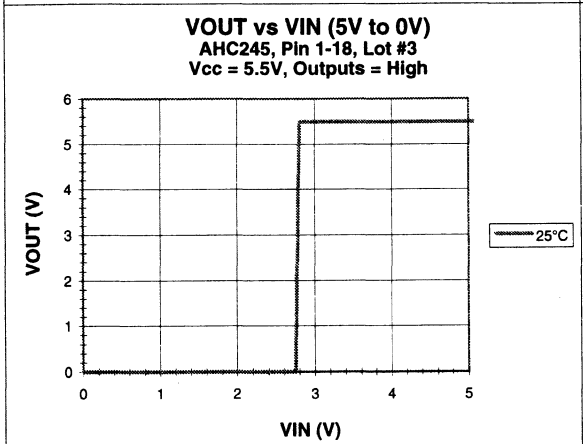

VOUT vs VIN (0V to 5V)
AHC245, Pin 1-18, Lot #2
Vcc = 5.5V, Outputs = High
VOUT (V)
VIN (V)
25°C

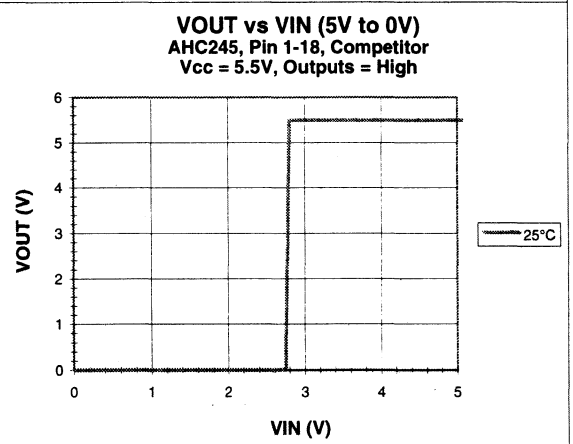

VOUT vs VIN (0V to 5V)
AHC245, Pin 1-18, Lot #3
Vcc = 5.5V, Outputs = High
VOUT (V)
VIN (V)
25°C

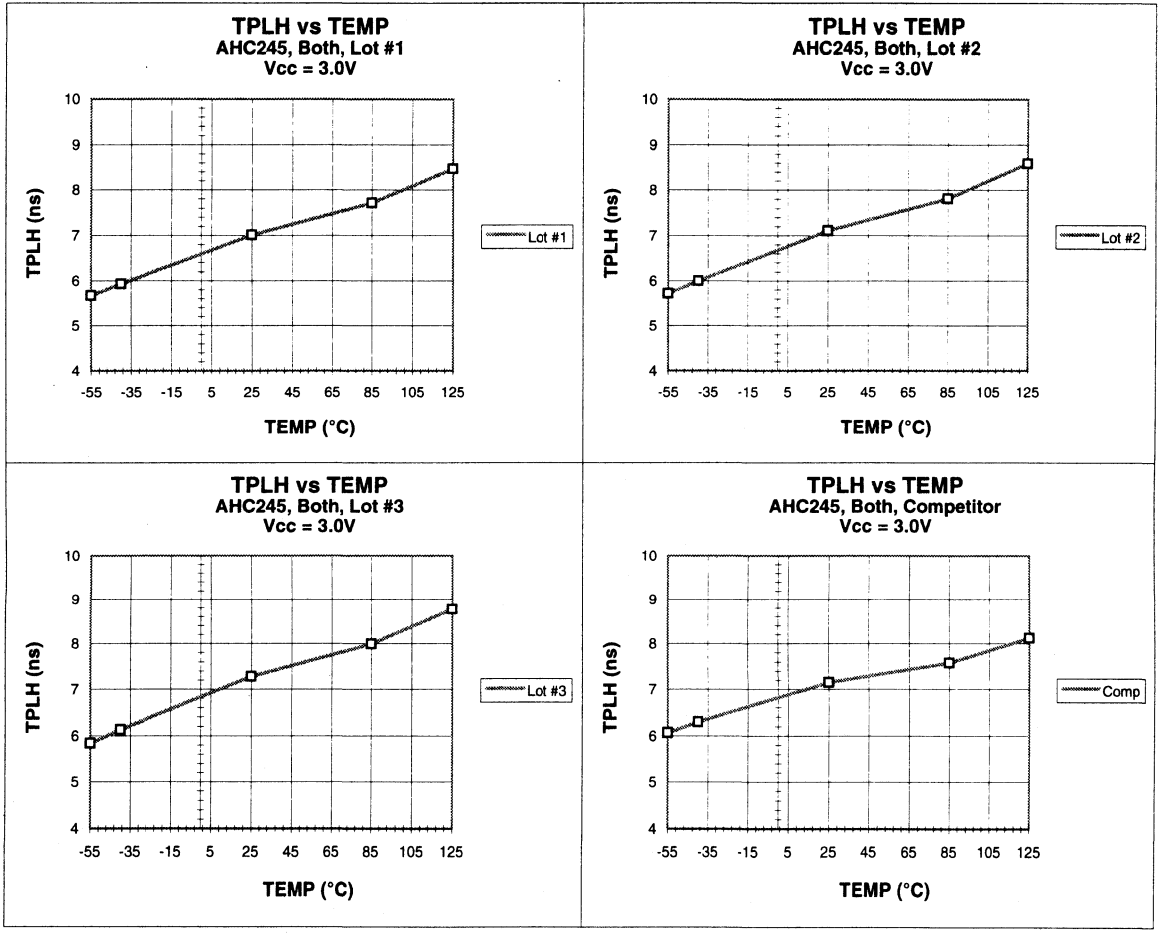

VOUT vs VIN (0V to 5V)
AHC245, Pin 1-18, Competitor
Vcc = 5.5V, Outputs = High
VOUT (V)
VIN (V)
25°C

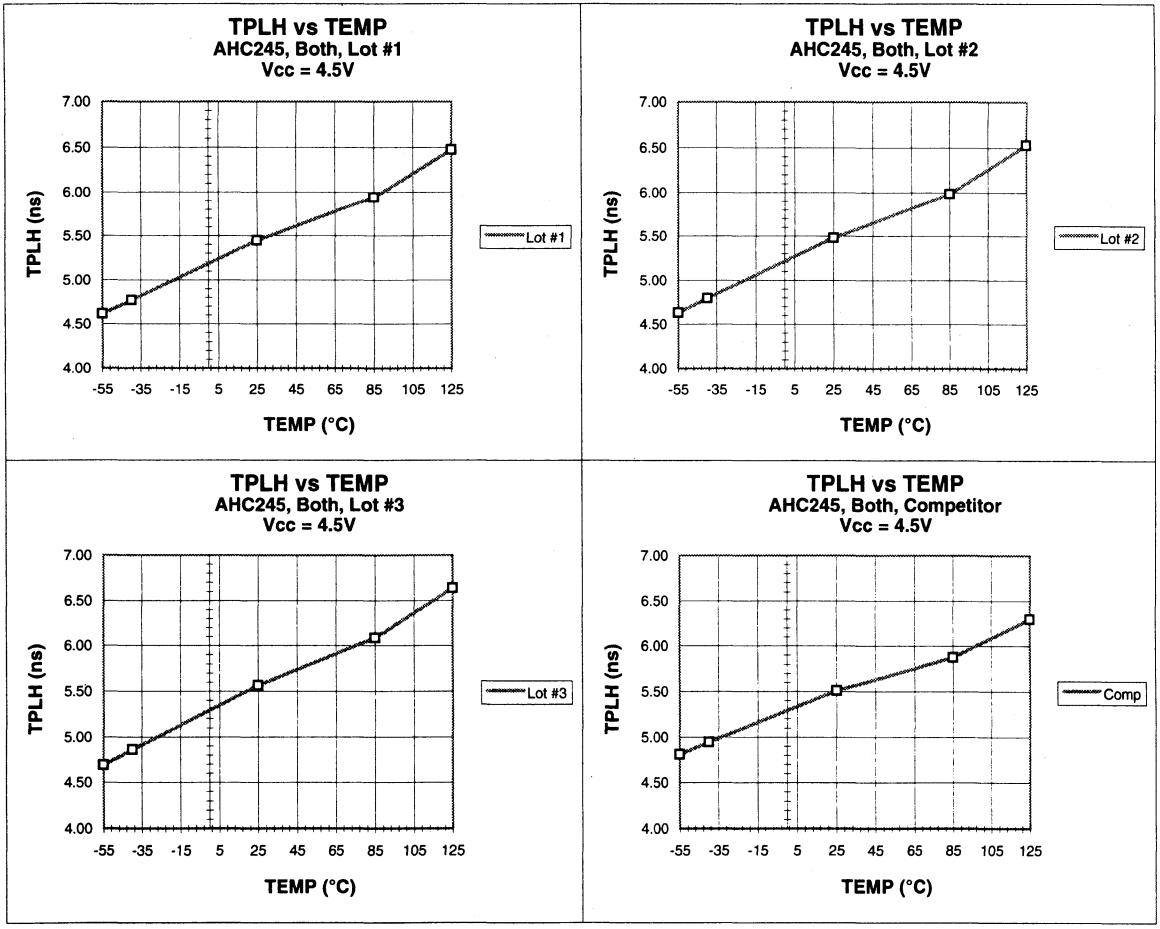

VOUT vs VIN (5V to 0V)
AHC245, Pin 1-18, Lot #1
Vcc = 5.5V, Outputs = High
VOUT (V)
VIN (V)
25°C

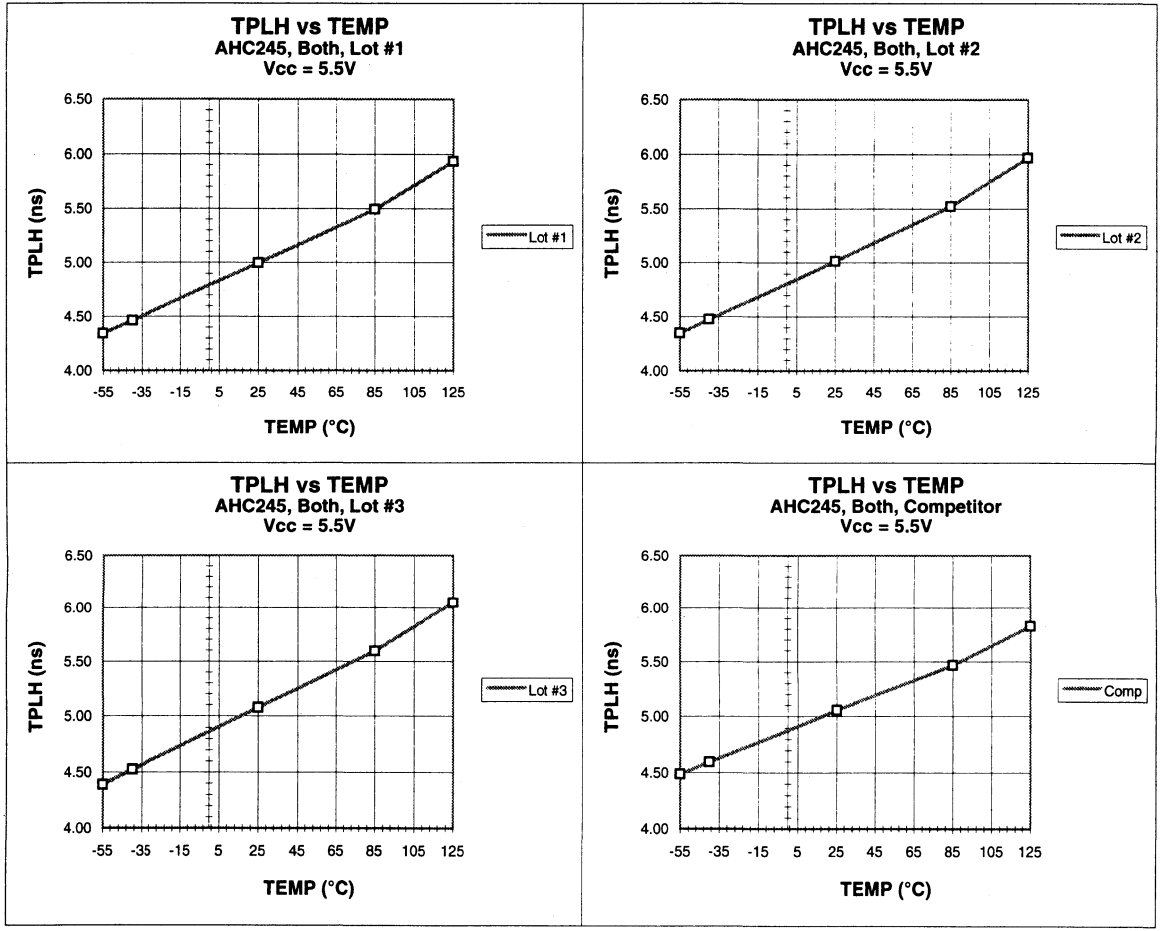

VOUT vs VIN (5V to 0V)
AHC245, Pin 1-18, Lot #2
Vcc = 5.5V, Outputs = High
VOUT (V)
VIN (V)
25°C

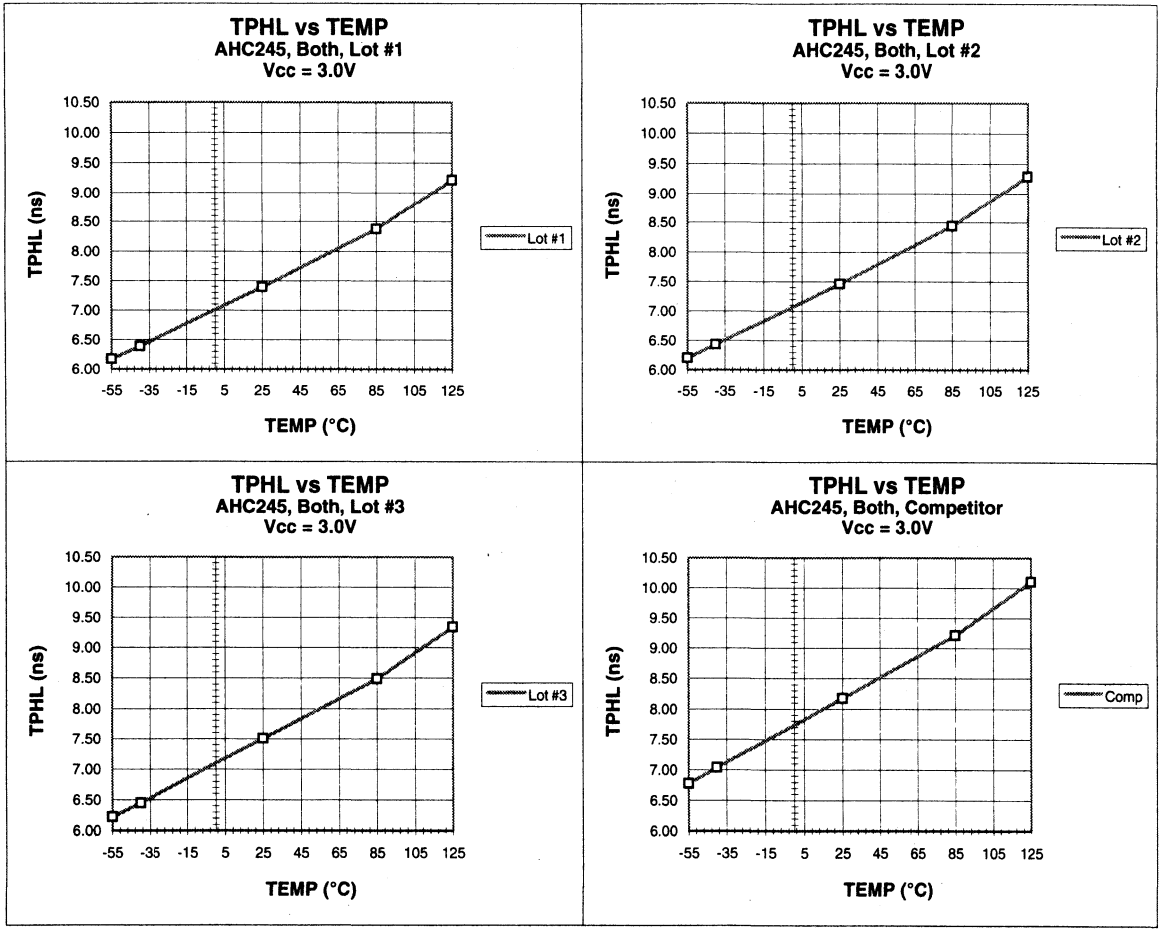

VOUT vs VIN (5V to 0V)
AHC245, Pin 1-18, Lot #3
Vcc = 5.5V, Outputs = High
VOUT (V)
VIN (V)
25°C

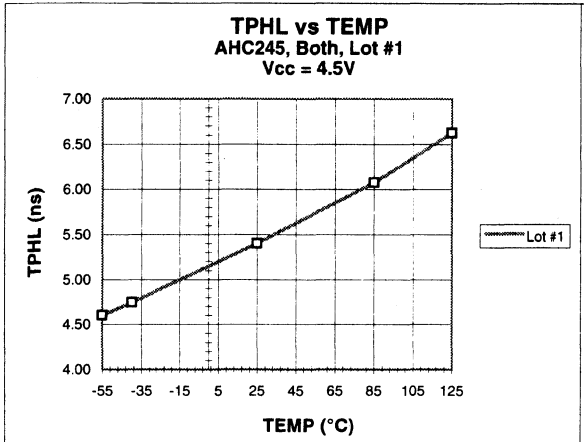

VOUT vs VIN (5V to 0V)
AHC245, Pin 1-18, Competitor
Vcc = 5.5V, Outputs = High
VOUT (V)
VIN (V)
25°C

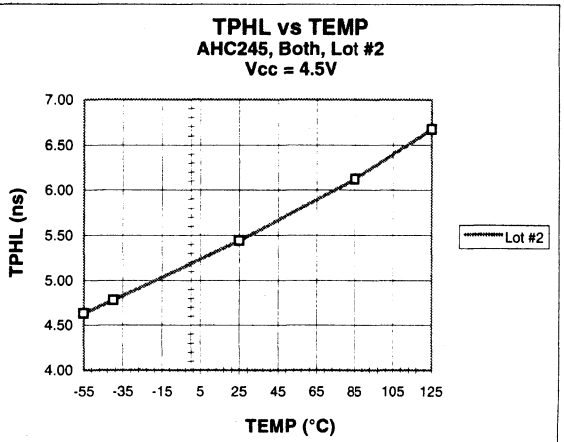

TPLH vs TEMP
AHC245, Both, Lot #1
Vcc = 3.0V
TPLH (ns)
10
9
8
7
6
5
4
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Lot #1
TPLH vs TEMP
AHC245, Both, Lot #2
Vcc = 3.0V
TPLH (ns)
10
9
8
7
6
5
4
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Lot #2
TPLH vs TEMP
AHC245, Both, Lot #3
Vcc = 3.0V
TPLH (ns)
10
9
8
7
6
5
4
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Lot #3
TPLH vs TEMP
AHC245, Both, Competitor
Vcc = 3.0V
TPLH (ns)
10
9
8
7
6
5
4
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Comp

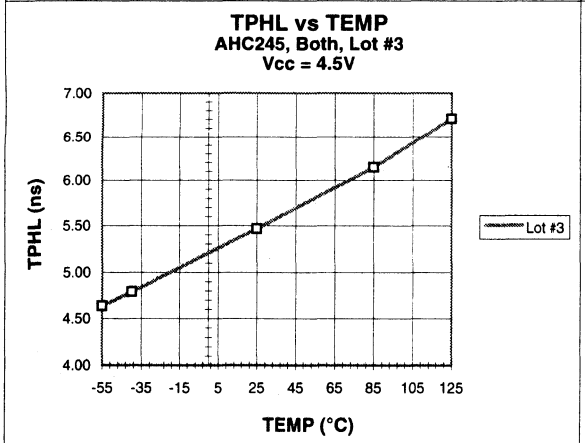

TPLH vs TEMP
AHC245, Both, Lot #1
Vcc = 4.5V
TPLH (ns)
7.00
6.50
6.00
5.50
5.00
4.50
4.00
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Lot #1
TPLH vs TEMP
AHC245, Both, Lot #2
Vcc = 4.5V
TPLH (ns)
7.00
6.50
6.00
5.50
5.00
4.50
4.00
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Lot #2
TPLH vs TEMP
AHC245, Both, Lot #3
Vcc = 4.5V
TPLH (ns)
7.00
6.50
6.00
5.50
5.00
4.50
4.00
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Lot #3
TPLH vs TEMP
AHC245, Both, Competitor
Vcc = 4.5V
TPLH (ns)
7.00
6.50
6.00
5.50
5.00
4.50
4.00
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Comp

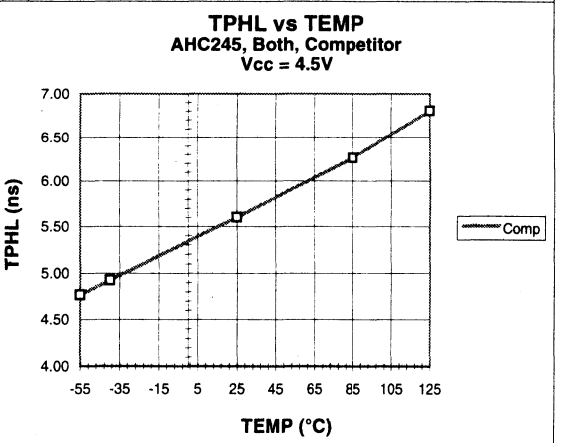

TPLH vs TEMP
AHC245, Both, Lot #1
Vcc = 5.5V
TPLH (ns)
6.50
6.00
5.50
5.00
4.50
4.00
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Lot #1
TPLH vs TEMP
AHC245, Both, Lot #2
Vcc = 5.5V
TPLH (ns)
6.50
6.00
5.50
5.00
4.50
4.00
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Lot #2
TPLH vs TEMP
AHC245, Both, Lot #3
Vcc = 5.5V
TPLH (ns)
6.50
6.00
5.50
5.00
4.50
4.00
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Lot #3
TPLH vs TEMP
AHC245, Both, Competitor
Vcc = 5.5V
TPLH (ns)
6.50
6.00
5.50
5.00
4.50
4.00
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Comp

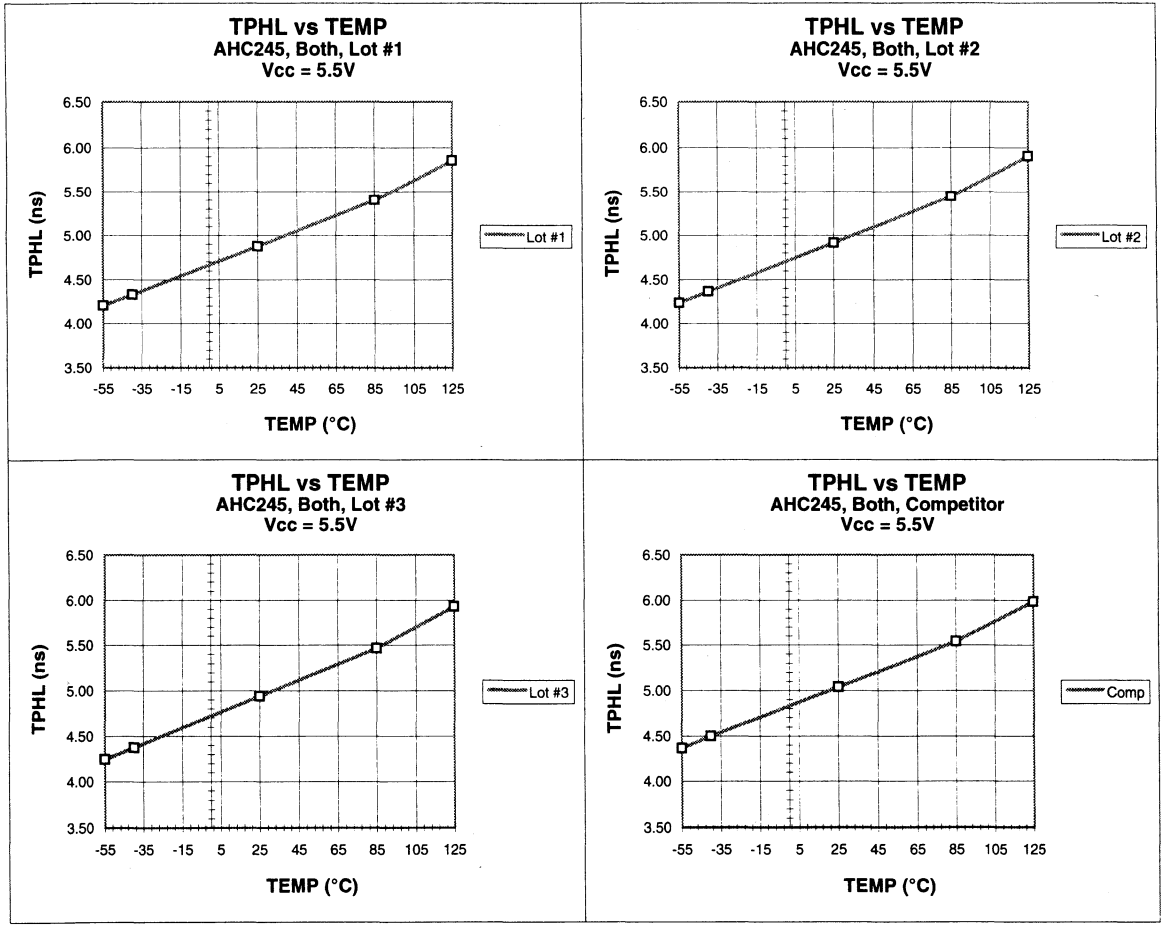

TPHL vs TEMP
AHC245, Both, Lot #1
Vcc = 3.0V
TPHL (ns)
10.50
10.00
9.50
9.00
8.50
8.00
7.50
7.00
6.50
6.00
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Lot #1
TPHL vs TEMP
AHC245, Both, Lot #2
Vcc = 3.0V
TPHL (ns)
10.50
10.00
9.50
9.00
8.50
8.00
7.50
7.00
6.50
6.00
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Lot #2
TPHL vs TEMP
AHC245, Both, Lot #3
Vcc = 3.0V
TPHL (ns)
10.50
10.00
9.50
9.00
8.50
8.00
7.50
7.00
6.50
6.00
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Lot #3
TPHL vs TEMP
AHC245, Both, Competitor
Vcc = 3.0V
TPHL (ns)
10.50
10.00
9.50
9.00
8.50
8.00
7.50
7.00
6.50
6.00
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Comp

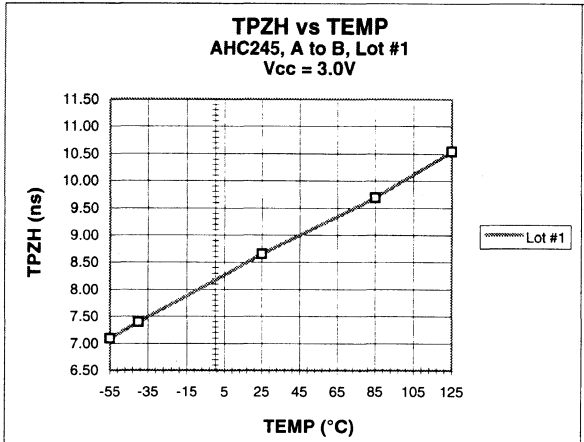

TPHL vs TEMP
AHC245, Both, Lot #1
Vcc = 4.5V
TPHL (ns)
7.00
6.50
6.00
5.50
5.00
4.50
4.00
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Lot #1

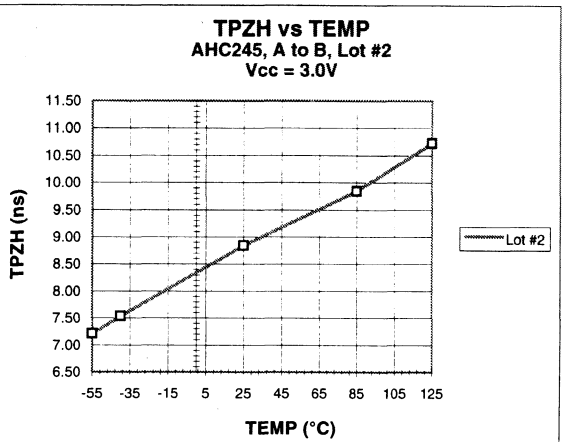

TPHL vs TEMP
AHC245, Both, Lot #2
Vcc = 4.5V
TPHL (ns)
7.00
6.50
6.00
5.50
5.00
4.50
4.00
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Lot #2

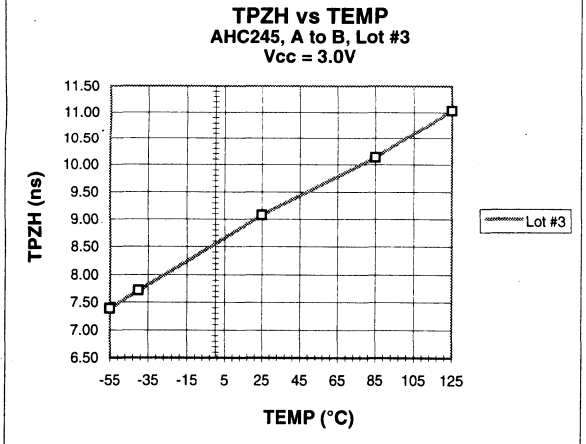

TPHL vs TEMP
AHC245, Both, Lot #3
Vcc = 4.5V
TPHL (ns)
7.00
6.50
6.00
5.50
5.00
4.50
4.00
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Lot #3

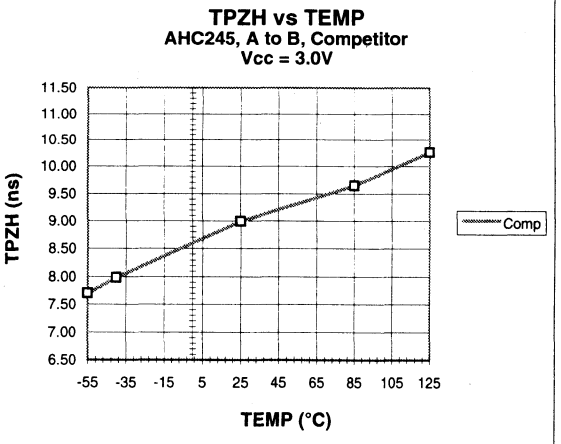

TPHL vs TEMP
AHC245, Both, Competitor
Vcc = 4.5V
TPHL (ns)
7.00
6.50
6.00
5.50
5.00
4.50
4.00
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Comp

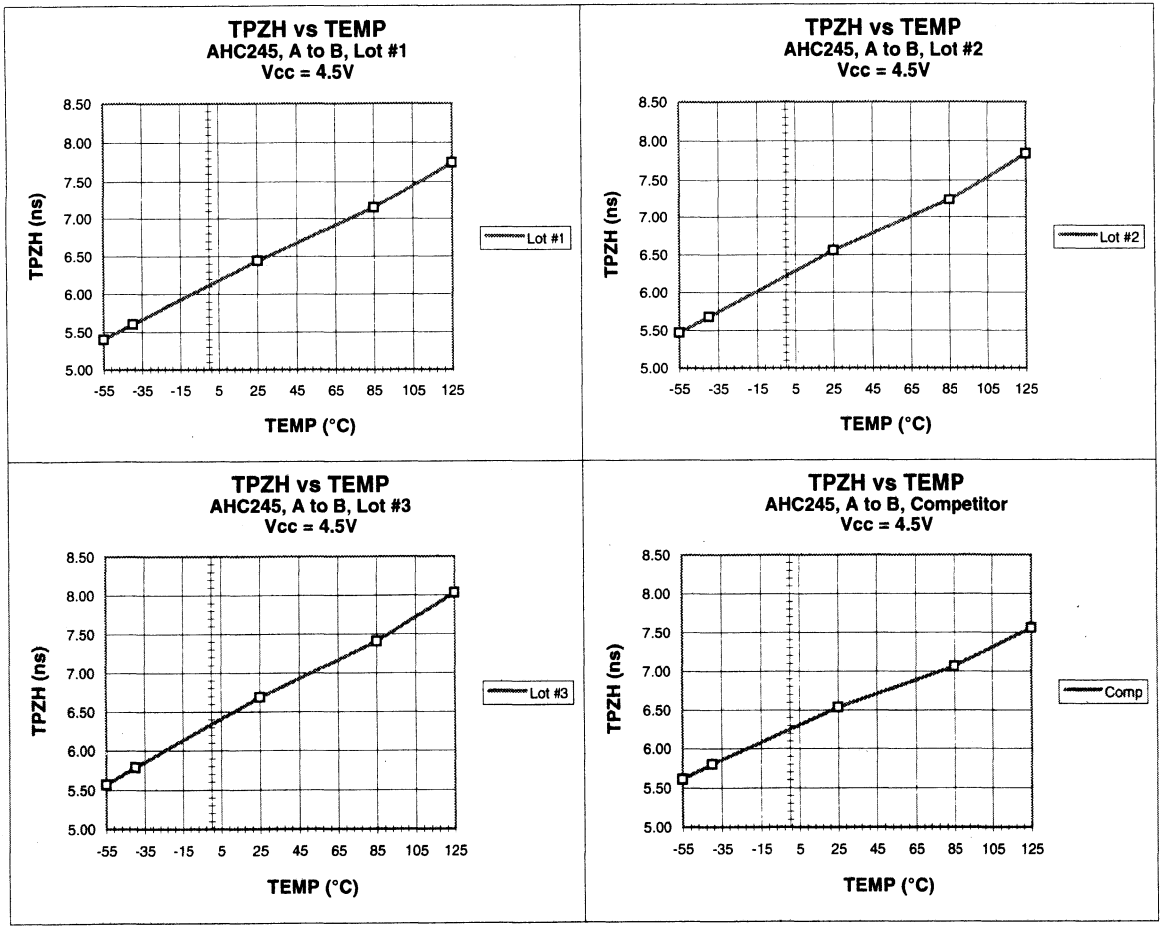

TPHL vs TEMP
AHC245, Both, Lot #1
Vcc = 5.5V
TPHL (ns)
6.50
6.00
5.50
5.00
4.50
4.00
3.50
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Lot #1
TPHL vs TEMP
AHC245, Both, Lot #2
Vcc = 5.5V
TPHL (ns)
6.50
6.00
5.50
5.00
4.50
4.00
3.50
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Lot #2
TPHL vs TEMP
AHC245, Both, Lot #3
Vcc = 5.5V
TPHL (ns)
6.50
6.00
5.50
5.00
4.50
4.00
3.50
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Lot #3
TPHL vs TEMP
AHC245, Both, Competitor
Vcc = 5.5V
TPHL (ns)
6.50
6.00
5.50
5.00
4.50
4.00
3.50
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Comp

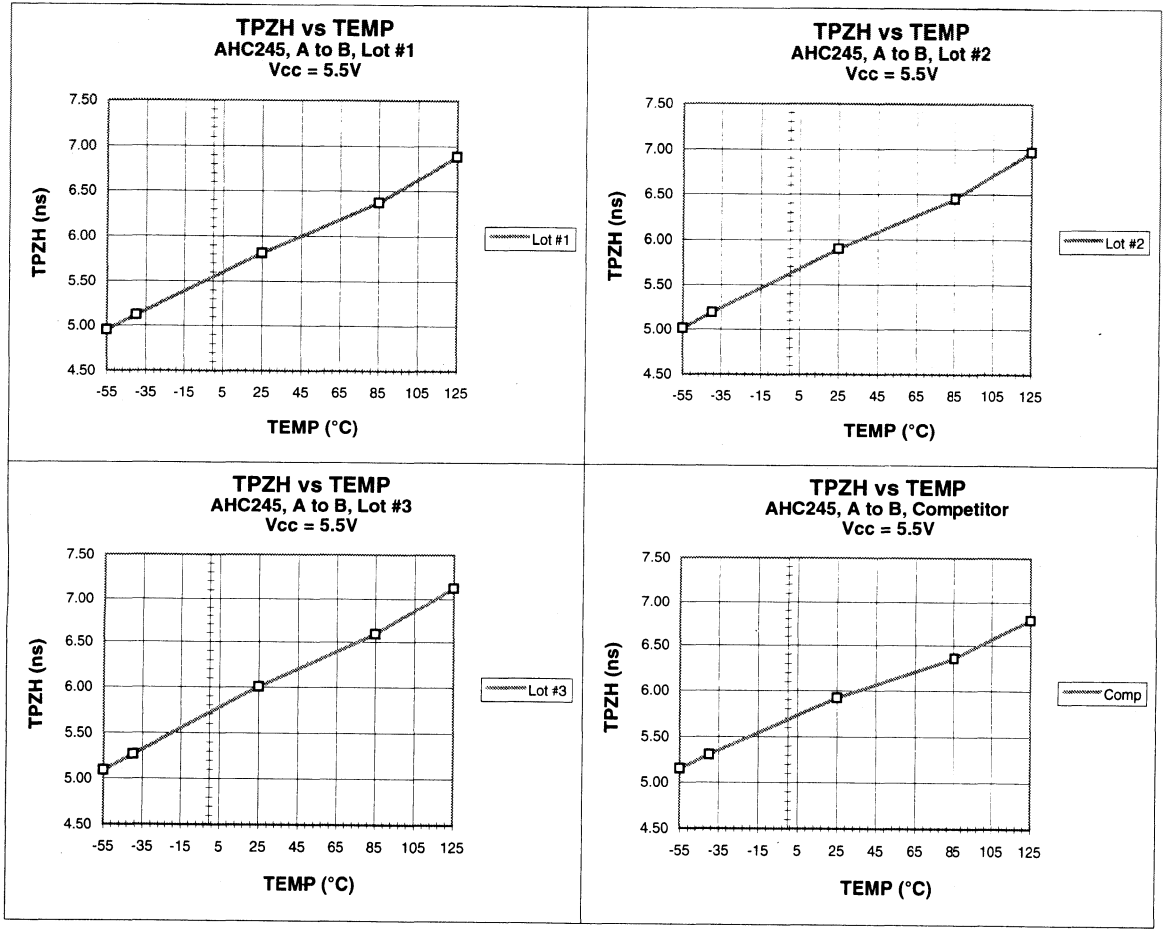

TPZH vs TEMP
AHC245, A to B, Lot #1
Vcc = 3.0V
TPZH (ns)
11.50
11.00
10.50
10.00
9.50
9.00
8.50
8.00
7.50
7.00
6.50
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Lot #1

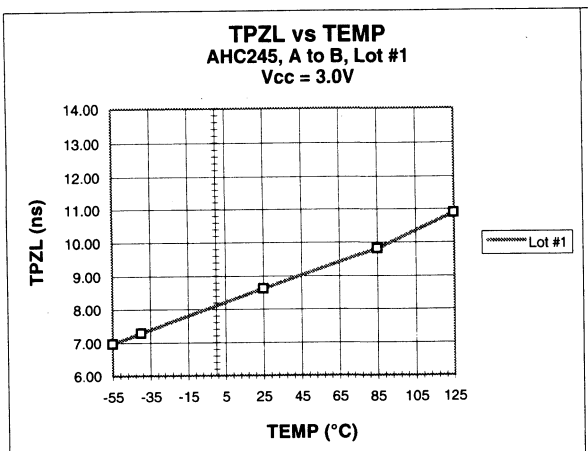

TPZH vs TEMP
AHC245, A to B, Lot #2
Vcc = 3.0V
TPZH (ns)
11.50
11.00
10.50
10.00
9.50
9.00
8.50
8.00
7.50
7.00
6.50
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Lot #2

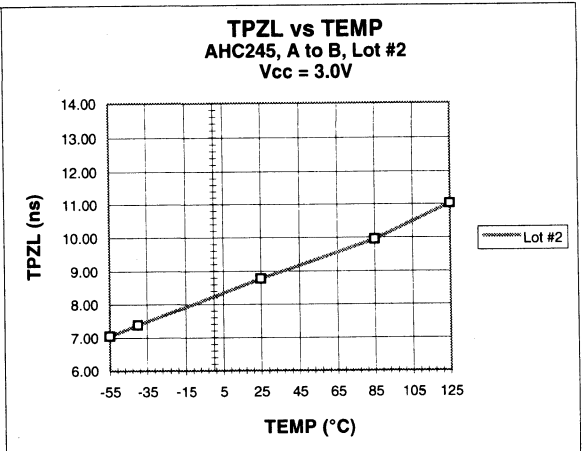

TPZH vs TEMP
AHC245, A to B, Lot #3
Vcc = 3.0V
TPZH (ns)
11.50
11.00
10.50
10.00
9.50
9.00
8.50
8.00
7.50
7.00
6.50
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Lot #3

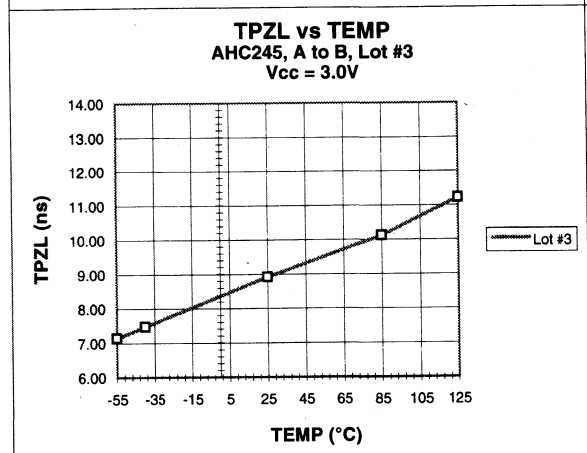

TPZH vs TEMP
AHC245, A to B, Competitor
Vcc = 3.0V
TPZH (ns)
11.50
11.00
10.50
10.00
9.50
9.00
8.50
8.00
7.50
7.00
6.50
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Comp

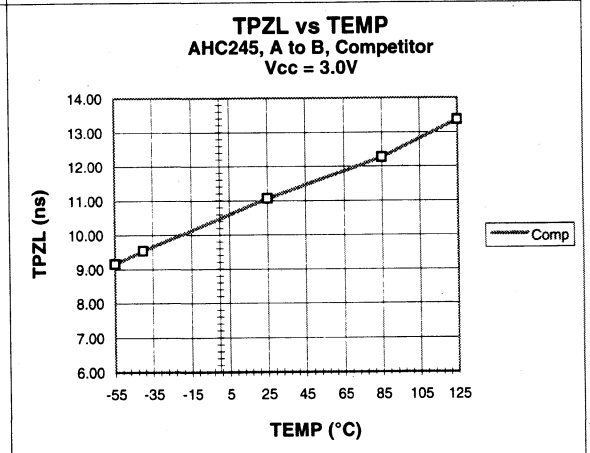

TPZH vs TEMP
AHC245, A to B, Lot #1
Vcc = 4.5V
TPZH (ns)
8.50
8.00
7.50
7.00
6.50
6.00
5.50
5.00
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Lot #1
TPZH vs TEMP
AHC245, A to B, Lot #2
Vcc = 4.5V
TPZH (ns)
8.50
8.00
7.50
7.00
6.50
6.00
5.50
5.00
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Lot #2
TPZH vs TEMP
AHC245, A to B, Lot #3
Vcc = 4.5V
TPZH (ns)
8.50
8.00
7.50
7.00
6.50
6.00
5.50
5.00
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Lot #3
TPZH vs TEMP
AHC245, A to B, Competitor
Vcc = 4.5V
TPZH (ns)
8.50
8.00
7.50
7.00
6.50
6.00
5.50
5.00
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Comp

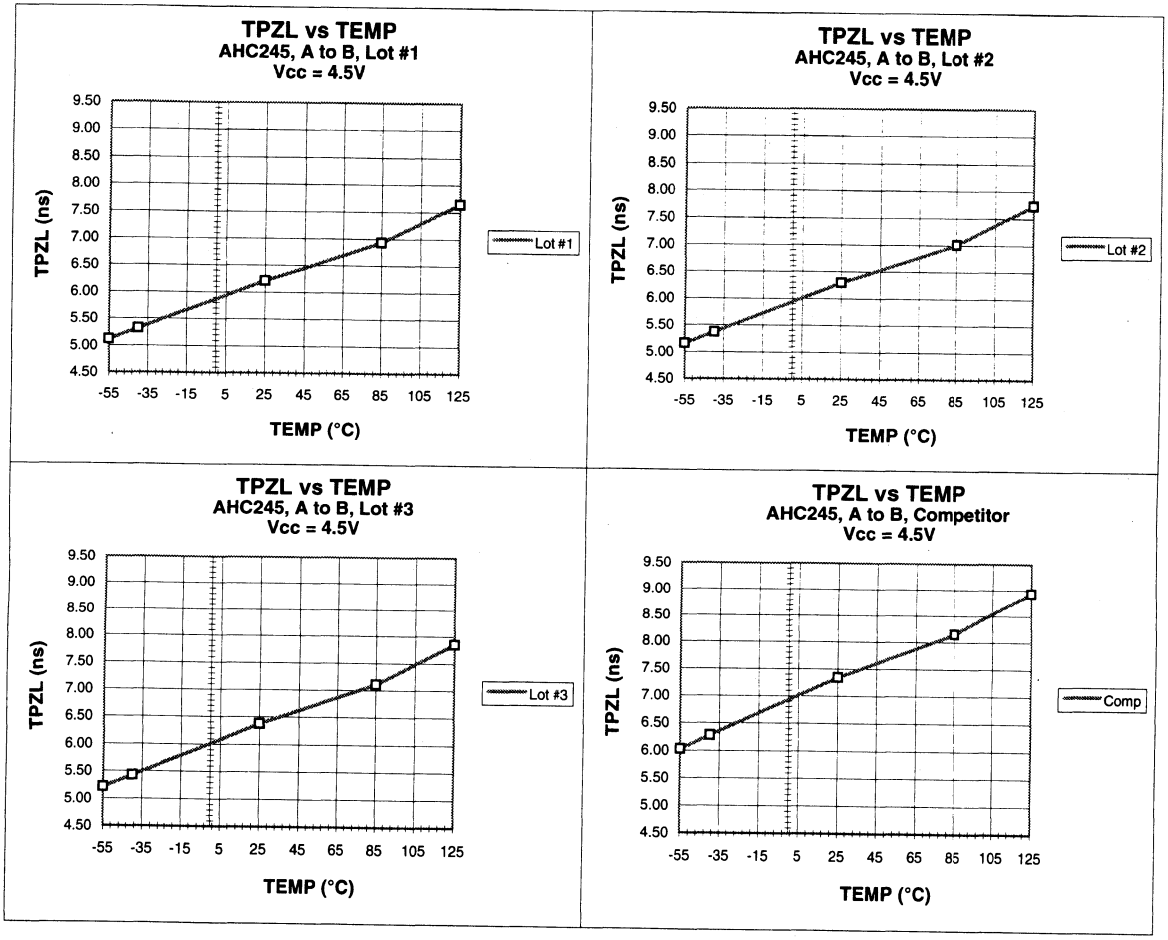

TPZH vs TEMP
AHC245, A to B, Lot #1
Vcc = 5.5V
TPZH (ns)
7.50
7.00
6.50
6.00
5.50
5.00
4.50
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Lot #1
TPZH vs TEMP
AHC245, A to B, Lot #2
Vcc = 5.5V
TPZH (ns)
7.50
7.00
6.50
6.00
5.50
5.00
4.50
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Lot #2
TPZH vs TEMP
AHC245, A to B, Lot #3
Vcc = 5.5V
TPZH (ns)
7.50
7.00
6.50
6.00
5.50
5.00
4.50
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Lot #3
TPZH vs TEMP
AHC245, A to B, Competitor
Vcc = 5.5V
TPZH (ns)
7.50
7.00
6.50
6.00
5.50
5.00
4.50
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Comp

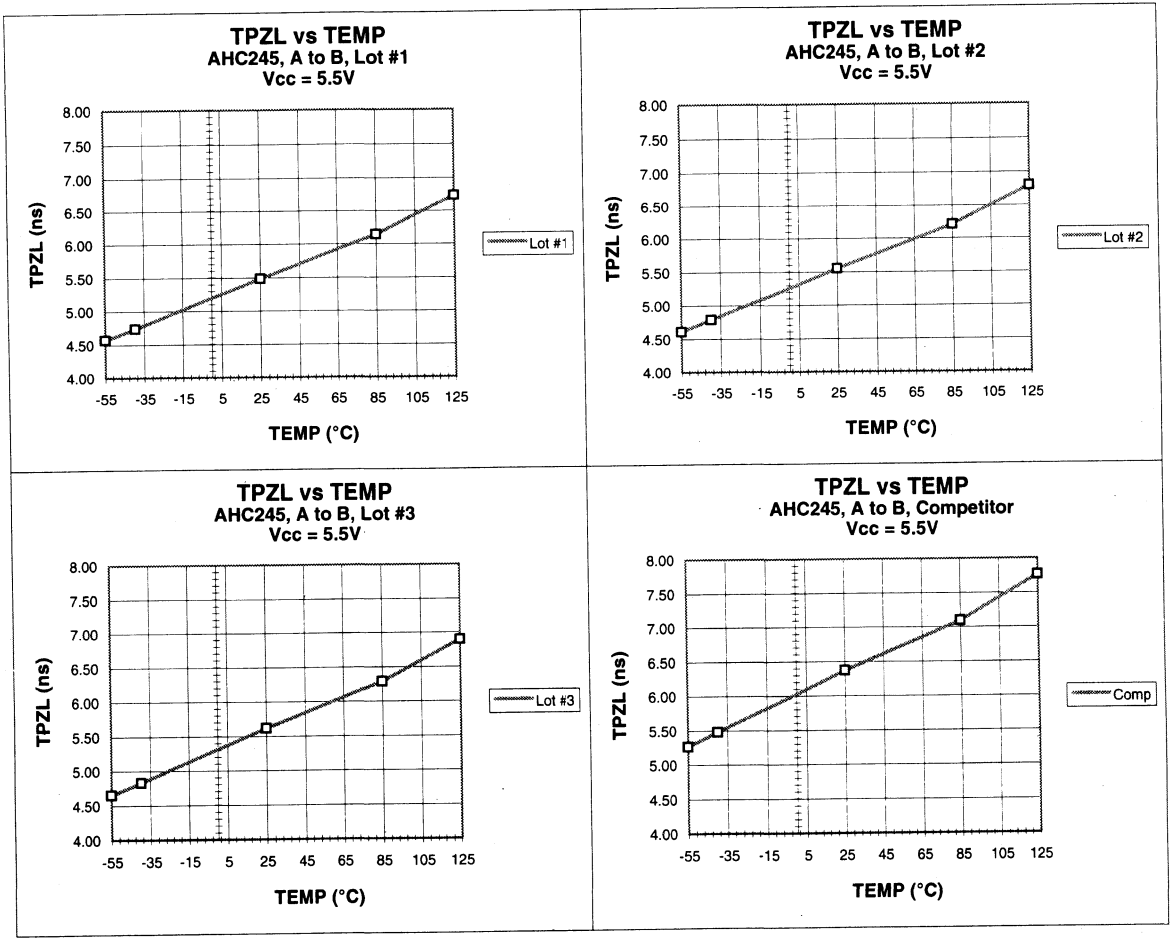

TPZL vs TEMP
AHC245, A to B, Lot #1
Vcc = 3.0V
TPZL (ns)
14.00
13.00
12.00
11.00
10.00
9.00
8.00
7.00
6.00
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Lot #1

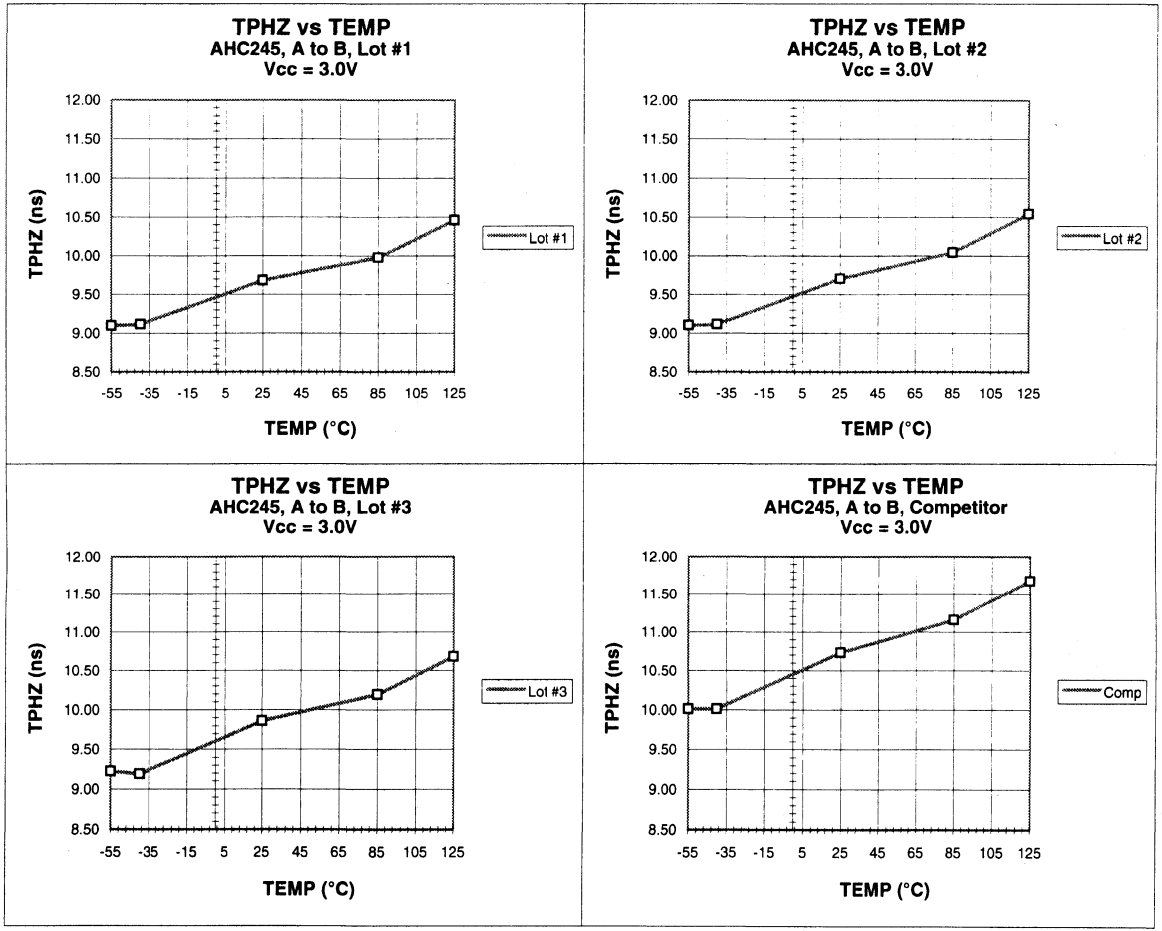

TPZL vs TEMP
AHC245, A to B, Lot #2
Vcc = 3.0V
TPZL (ns)
14.00
13.00
12.00
11.00
10.00
9.00
8.00
7.00
6.00
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Lot #2

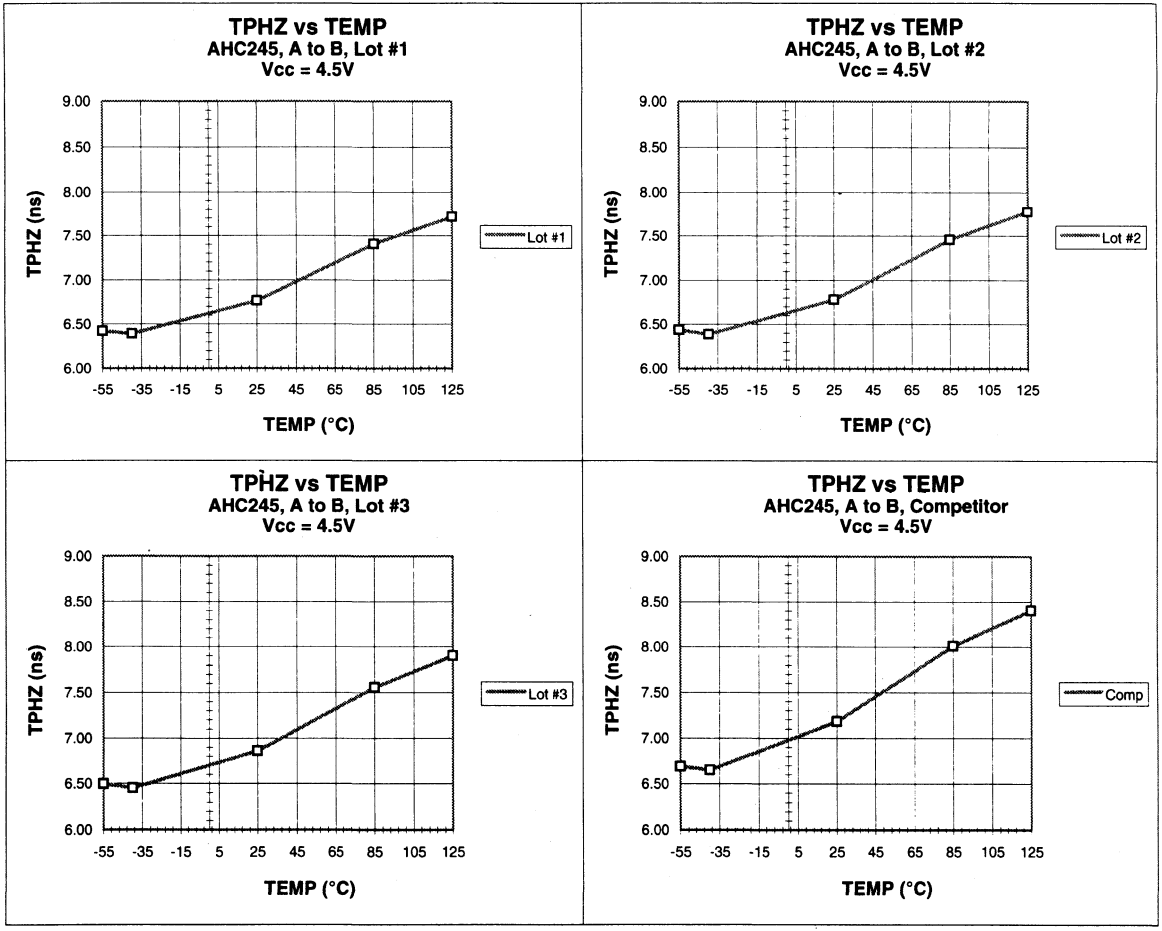

TPZL vs TEMP
AHC245, A to B, Lot #3
Vcc = 3.0V
TPZL (ns)
14.00
13.00
12.00
11.00
10.00
9.00
8.00
7.00
6.00
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Lot #3

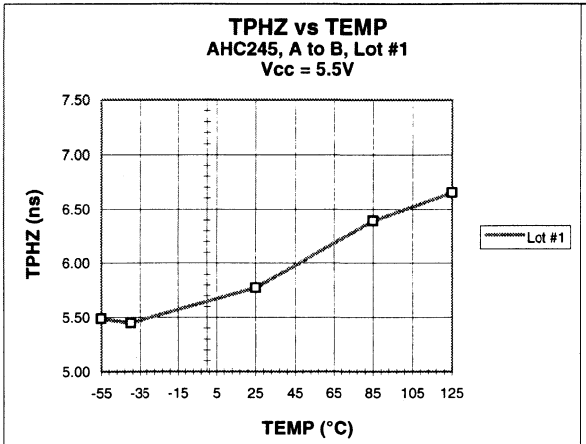

TPZL vs TEMP
AHC245, A to B, Competitor
Vcc = 3.0V
TPZL (ns)
14.00
13.00
12.00
11.00
10.00
9.00
8.00
7.00
6.00
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Comp

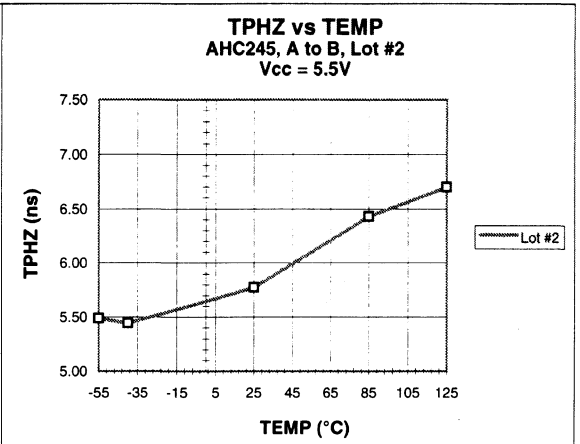

TPZL vs TEMP
AHC245, A to B, Lot #1
Vcc = 4.5V
TPZL (ns)
9.50
9.00
8.50
8.00
7.50
7.00
6.50
6.00
5.50
5.00
4.50
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Lot #1
TPZL vs TEMP
AHC245, A to B, Lot #2
Vcc = 4.5V
TPZL (ns)
9.50
9.00
8.50
8.00
7.50
7.00
6.50
6.00
5.50
5.00
4.50
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Lot #2
TPZL vs TEMP
AHC245, A to B, Lot #3
Vcc = 4.5V
TPZL (ns)
9.50
9.00
8.50
8.00
7.50
7.00
6.50
6.00
5.50
5.00
4.50
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Lot #3
TPZL vs TEMP
AHC245, A to B, Competitor
Vcc = 4.5V
TPZL (ns)
9.50
9.00
8.50
8.00
7.50
7.00
6.50
6.00
5.50
5.00
4.50
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Comp

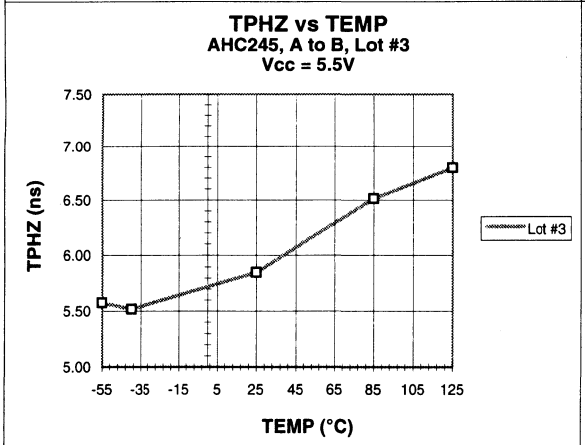

TPZL vs TEMP
AHC245, A to B, Lot #1
Vcc = 5.5V
TPZL (ns)
8.00
7.50
7.00
6.50
6.00
5.50
5.00
4.50
4.00
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Lot #1
TPZL vs TEMP
AHC245, A to B, Lot #2
Vcc = 5.5V
TPZL (ns)
8.00
7.50
7.00
6.50
6.00
5.50
5.00
4.50
4.00
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Lot #2
TPZL vs TEMP
AHC245, A to B, Lot #3
Vcc = 5.5V
TPZL (ns)
8.00
7.50
7.00
6.50
6.00
5.50
5.00
4.50
4.00
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Lot #3
TPZL vs TEMP
AHC245, A to B, Competitor
Vcc = 5.5V
TPZL (ns)
8.00
7.50
7.00
6.50
6.00
5.50
5.00
4.50
4.00
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Comp

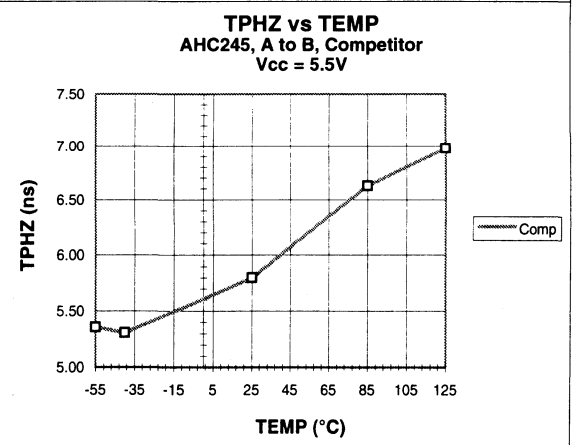

TPHZ vs TEMP
AHC245, A to B, Lot #1
Vcc = 3.0V
TPHZ (ns)
12.00
11.50
11.00
10.50
10.00
9.50
9.00
8.50
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Lot #1
TPHZ vs TEMP
AHC245, A to B, Lot #2
Vcc = 3.0V
TPHZ (ns)
12.00
11.50
11.00
10.50
10.00
9.50
9.00
8.50
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Lot #2
TPHZ vs TEMP
AHC245, A to B, Lot #3
Vcc = 3.0V
TPHZ (ns)
12.00
11.50
11.00
10.50
10.00
9.50
9.00
8.50
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Lot #3
TPHZ vs TEMP
AHC245, A to B, Competitor
Vcc = 3.0V
TPHZ (ns)
12.00
11.50
11.00
10.50
10.00
9.50
9.00
8.50
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Comp

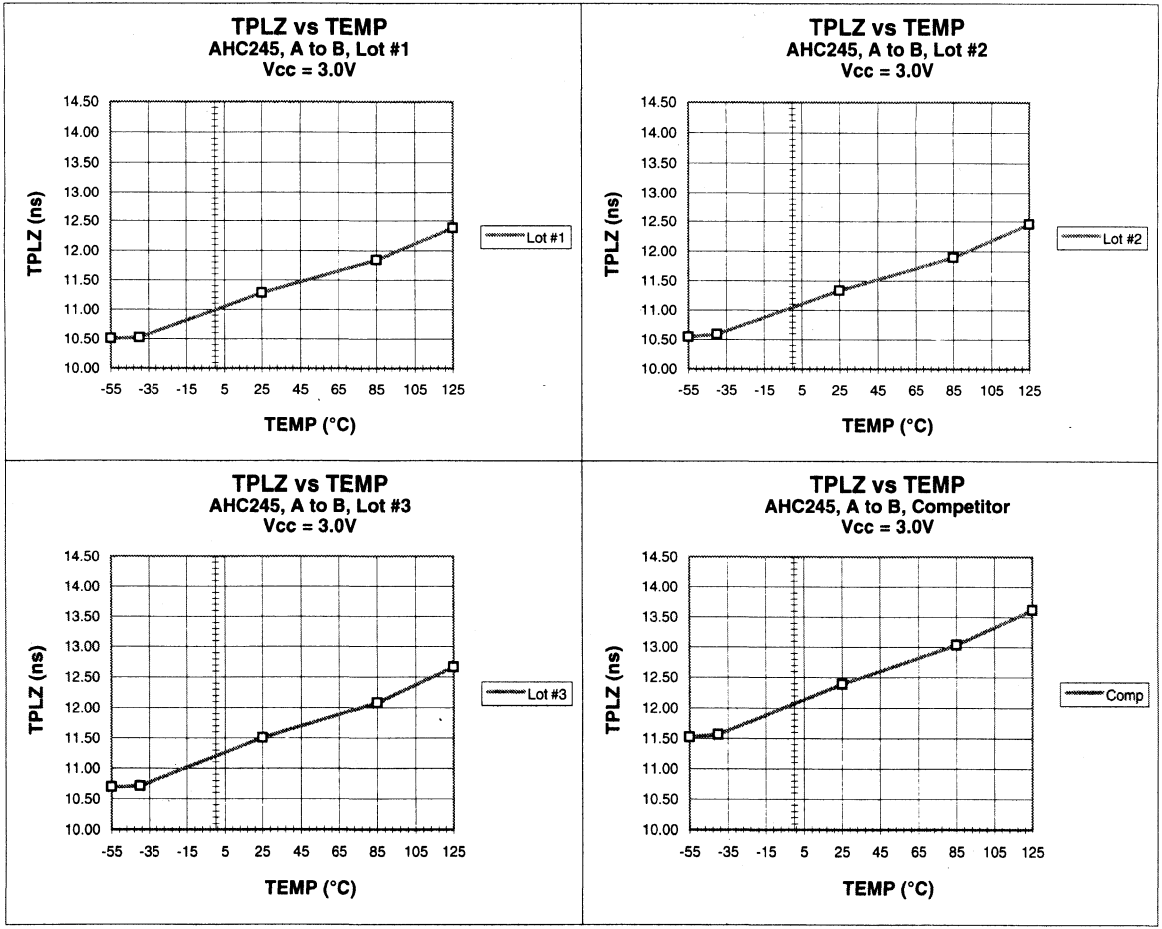

TPHZ vs TEMP
AHC245, A to B, Lot #1
Vcc = 4.5V
TPHZ (ns)
9.00
8.50
8.00
7.50
7.00
6.50
6.00
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Lot #1
TPHZ vs TEMP
AHC245, A to B, Lot #2
Vcc = 4.5V
TPHZ (ns)
9.00
8.50
8.00
7.50
7.00
6.50
6.00
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Lot #2
TPHZ vs TEMP
AHC245, A to B, Lot #3
Vcc = 4.5V
TPHZ (ns)
9.00
8.50
8.00
7.50
7.00
6.50
6.00
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Lot #3
TPHZ vs TEMP
AHC245, A to B, Competitor
Vcc = 4.5V
TPHZ (ns)
9.00
8.50
8.00
7.50
7.00
6.50
6.00
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Comp

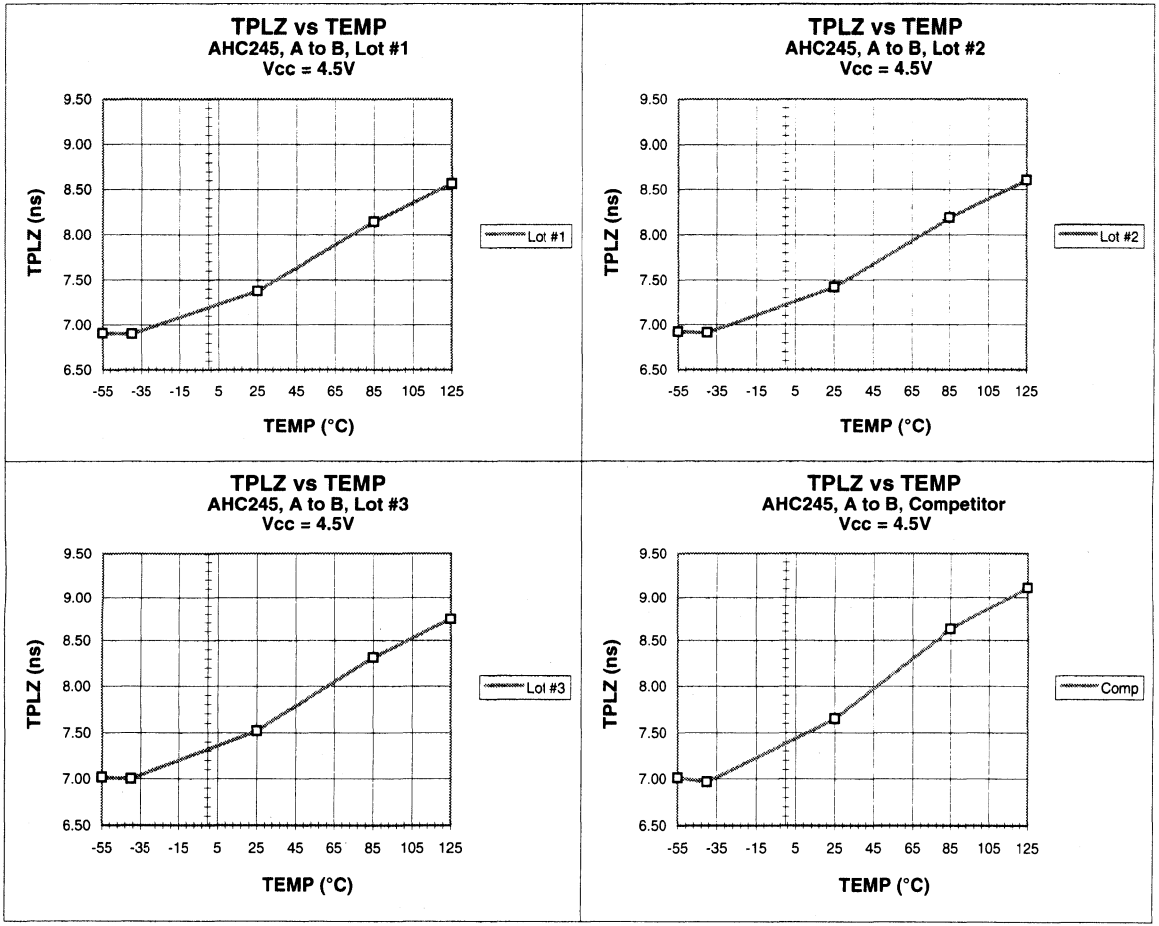

TPHZ vs TEMP
AHC245, A to B, Lot #1
Vcc = 5.5V
TPHZ (ns)
7.50
7.00
6.50
6.00
5.50
5.00
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Lot #1


TPHZ vs TEMP
AHC245, A to B, Lot #2
Vcc = 5.5V
TPHZ (ns)
7.50
7.00
6.50
6.00
5.50
5.00
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Lot #2


TPHZ vs TEMP
AHC245, A to B, Lot #3
Vcc = 5.5V
TPHZ (ns)
7.50
7.00
6.50
6.00
5.50
5.00
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Lot #3


TPHZ vs TEMP
AHC245, A to B, Competitor
Vcc = 5.5V
TPHZ (ns)
7.50
7.00
6.50
6.00
5.50
5.00
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Comp


TPLZ vs TEMP
AHC245, A to B, Lot #1
Vcc = 3.0V
TPLZ (ns)
14.50
14.00
13.50
13.00
12.50
12.00
11.50
11.00
10.50
10.00
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Lot #1
TPLZ vs TEMP
AHC245, A to B, Lot #2
Vcc = 3.0V
TPLZ (ns)
14.50
14.00
13.50
13.00
12.50
12.00
11.50
11.00
10.50
10.00
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Lot #2
TPLZ vs TEMP
AHC245, A to B, Lot #3
Vcc = 3.0V
TPLZ (ns)
14.50
14.00
13.50
13.00
12.50
12.00
11.50
11.00
10.50
10.00
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Lot #3
TPLZ vs TEMP
AHC245, A to B, Competitor
Vcc = 3.0V
TPLZ (ns)
14.50
14.00
13.50
13.00
12.50
12.00
11.50
11.00
10.50
10.00
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Comp


TPLZ vs TEMP
AHC245, A to B, Lot #1
Vcc = 4.5V
TPLZ (ns)
9.50
9.00
8.50
8.00
7.50
7.00
6.50
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Lot #1
TPLZ vs TEMP
AHC245, A to B, Lot #2
Vcc = 4.5V
TPLZ (ns)
9.50
9.00
8.50
8.00
7.50
7.00
6.50
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Lot #2
TPLZ vs TEMP
AHC245, A to B, Lot #3
Vcc = 4.5V
TPLZ (ns)
9.50
9.00
8.50
8.00
7.50
7.00
6.50
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Lot #3
TPLZ vs TEMP
AHC245, A to B, Competitor
Vcc = 4.5V
TPLZ (ns)
9.50
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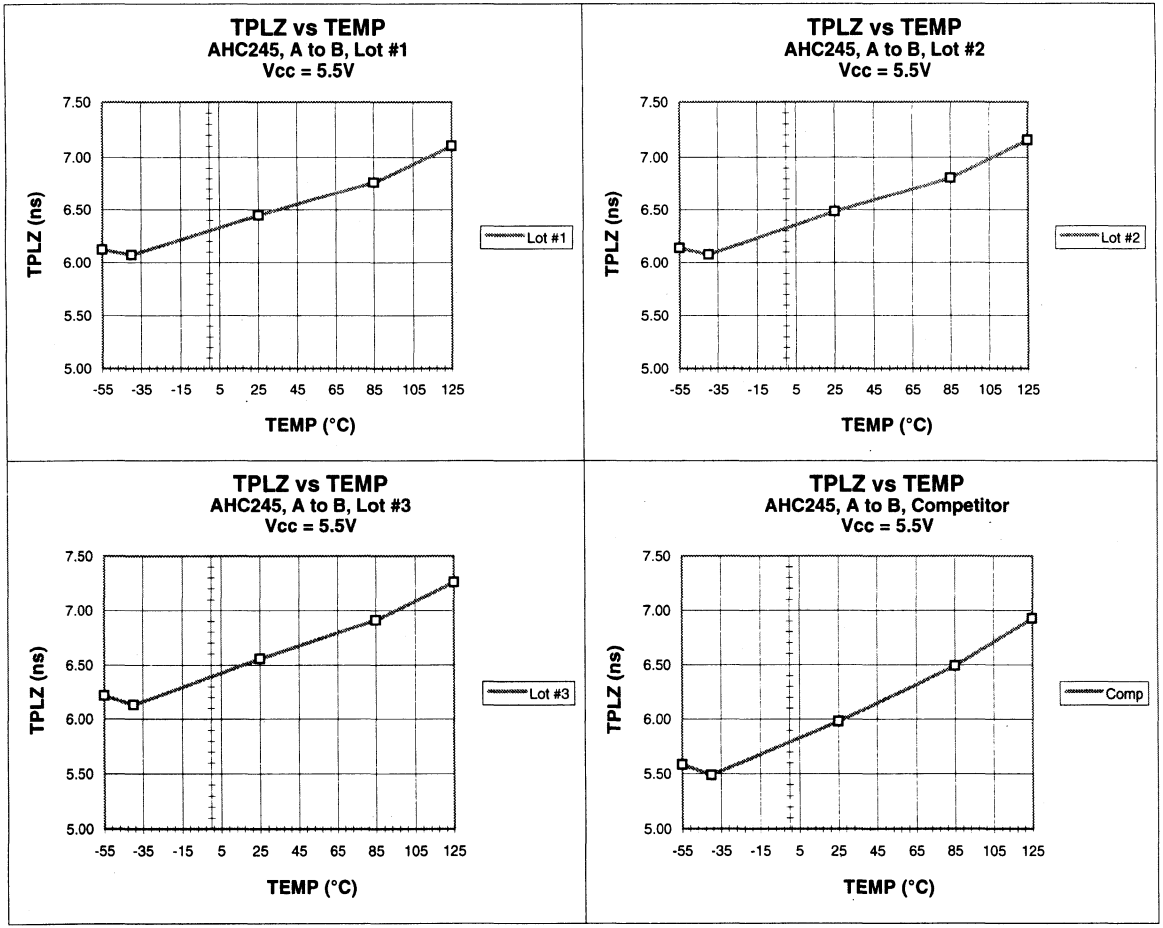
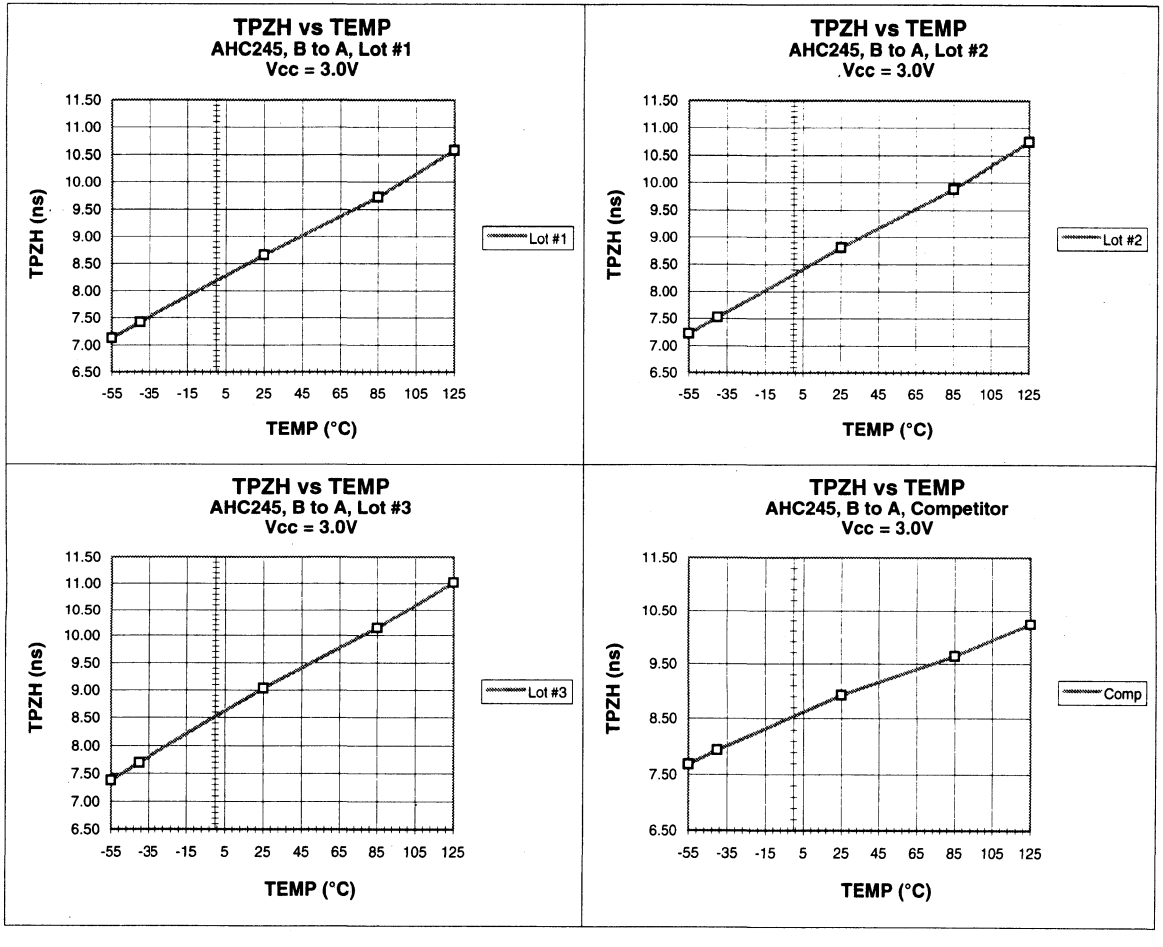
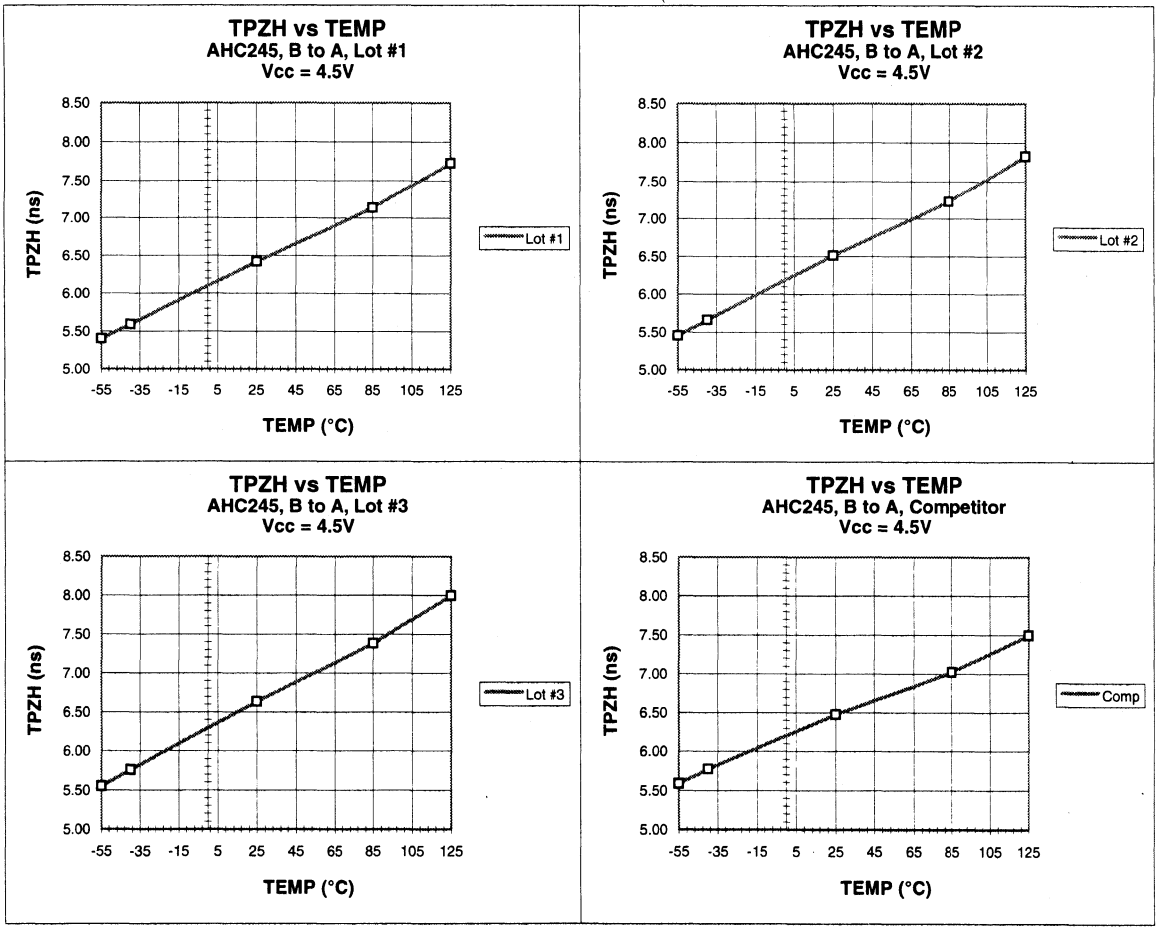
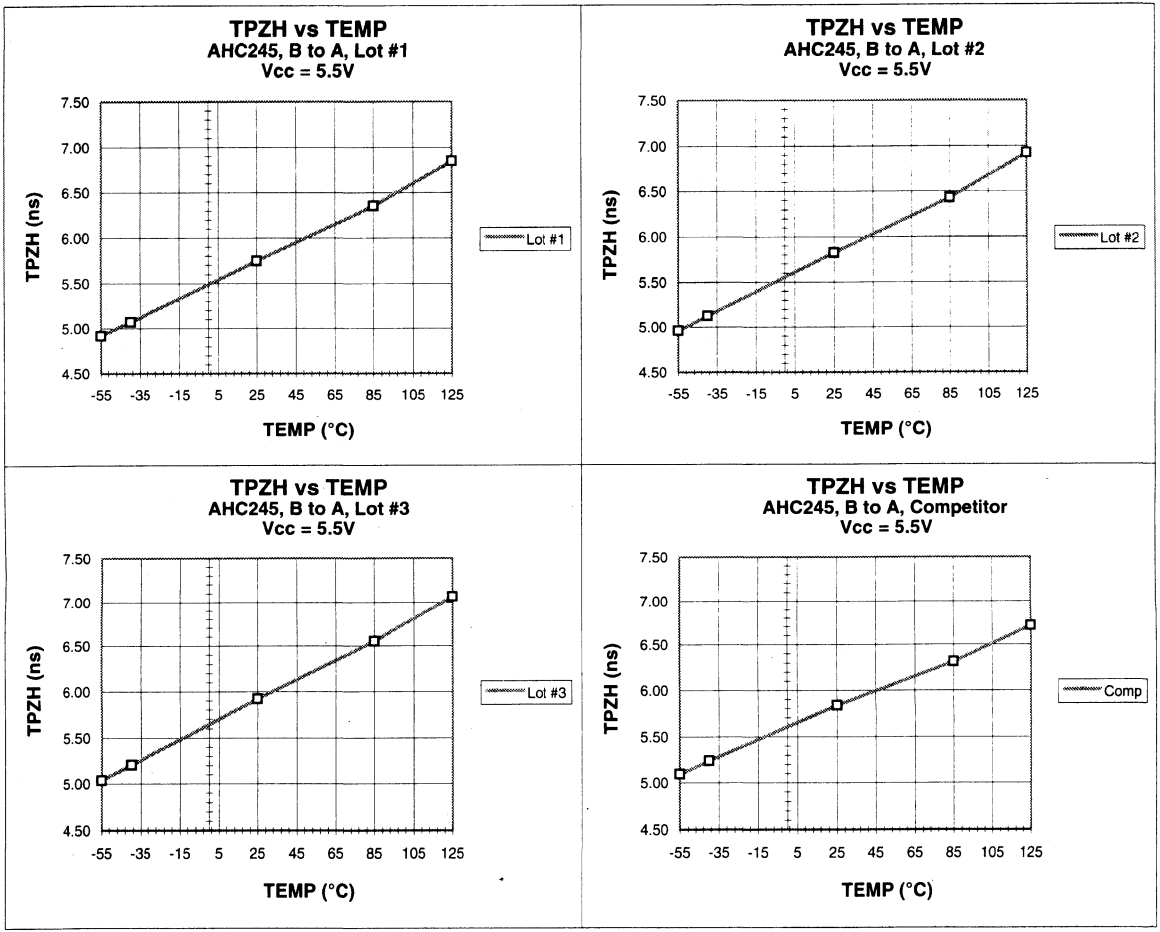
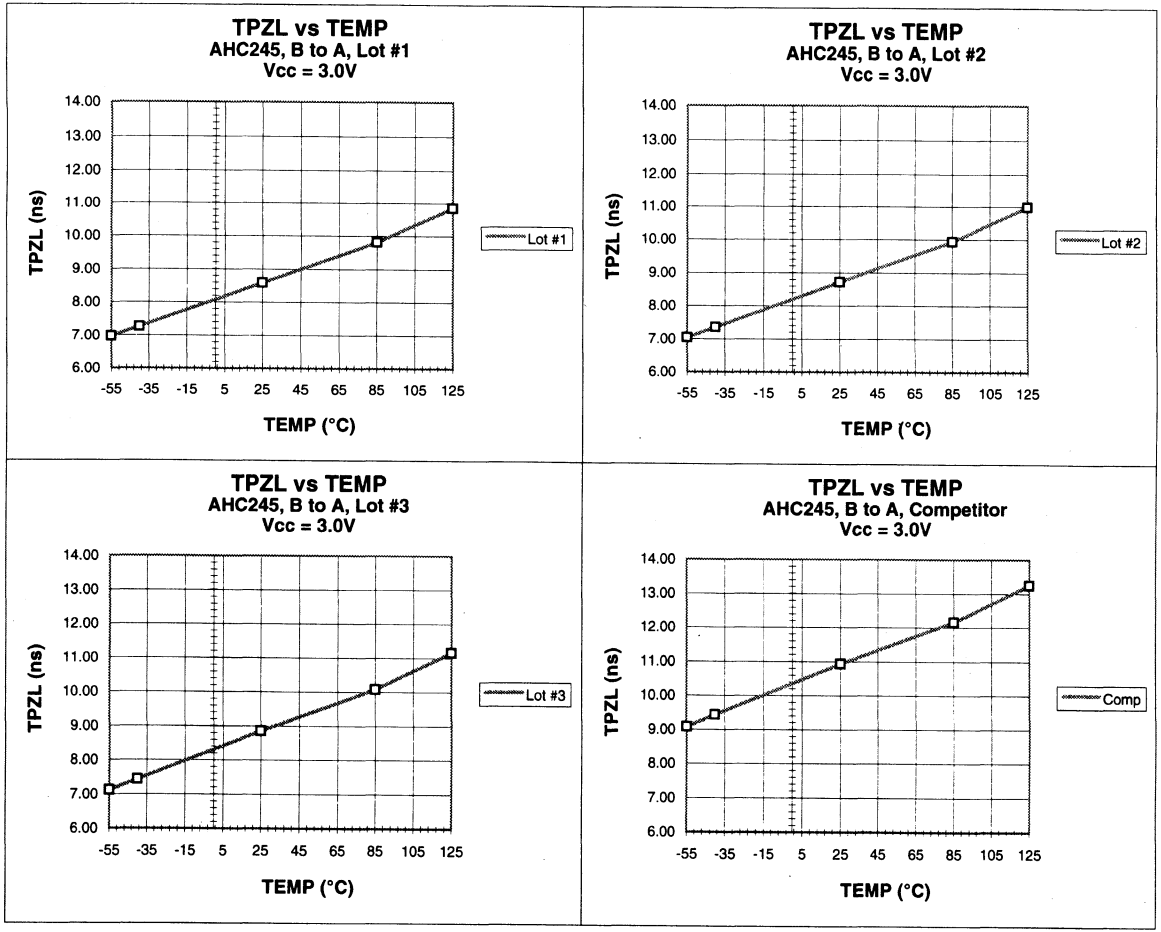
8.00
7.50
7.00
6.50
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Comp

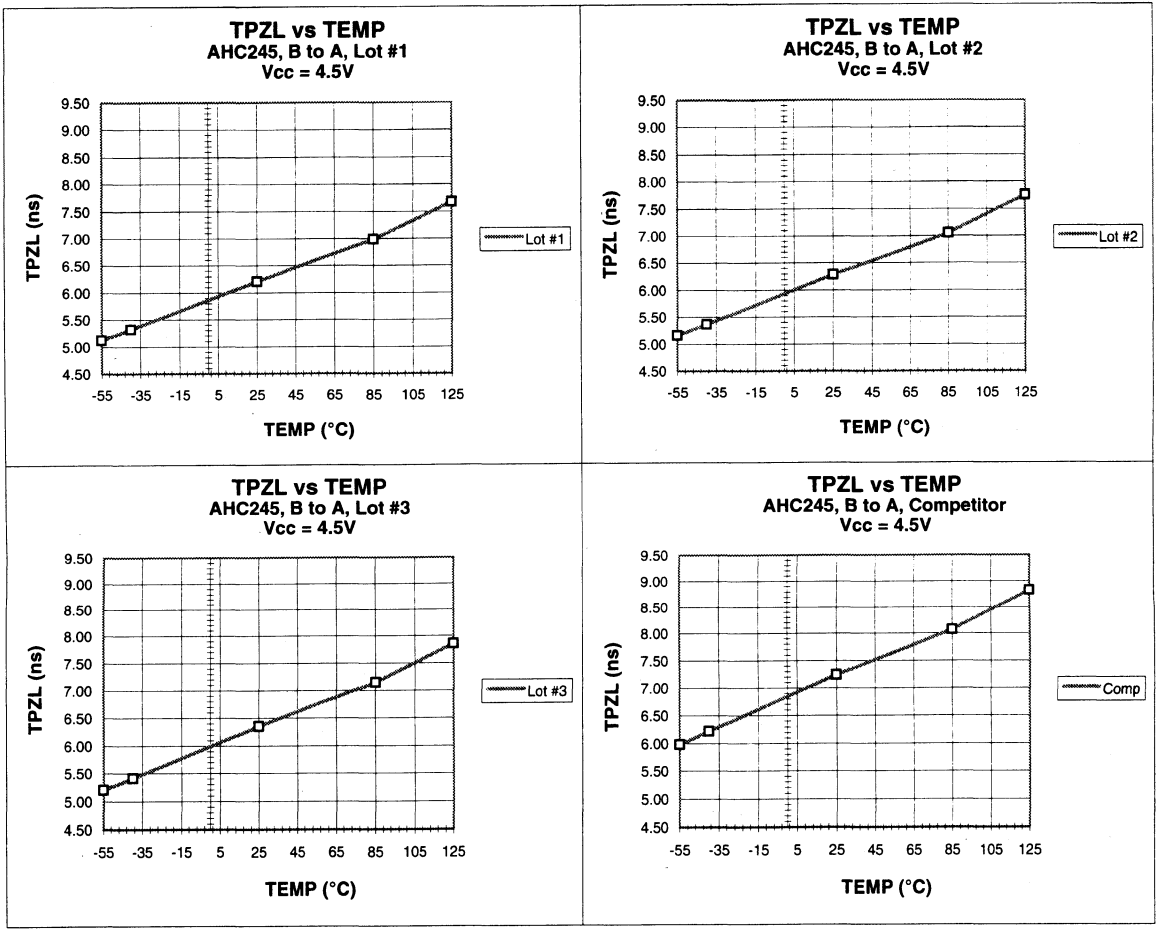

TPLZ vs TEMP
AHC245, A to B, Lot #1
Vcc = 5.5V
TPLZ (ns)
7.50
7.00
6.50
6.00
5.50
5.00
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Lot #1
TPLZ vs TEMP
AHC245, A to B, Lot #2
Vcc = 5.5V
TPLZ (ns)
7.50
7.00
6.50
6.00
5.50
5.00
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Lot #2
TPLZ vs TEMP
AHC245, A to B, Lot #3
Vcc = 5.5V
TPLZ (ns)
7.50
7.00
6.50
6.00
5.50
5.00
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Lot #3
TPLZ vs TEMP
AHC245, A to B, Competitor
Vcc = 5.5V
TPLZ (ns)
7.50
7.00
6.50
6.00
5.50
5.00
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Comp

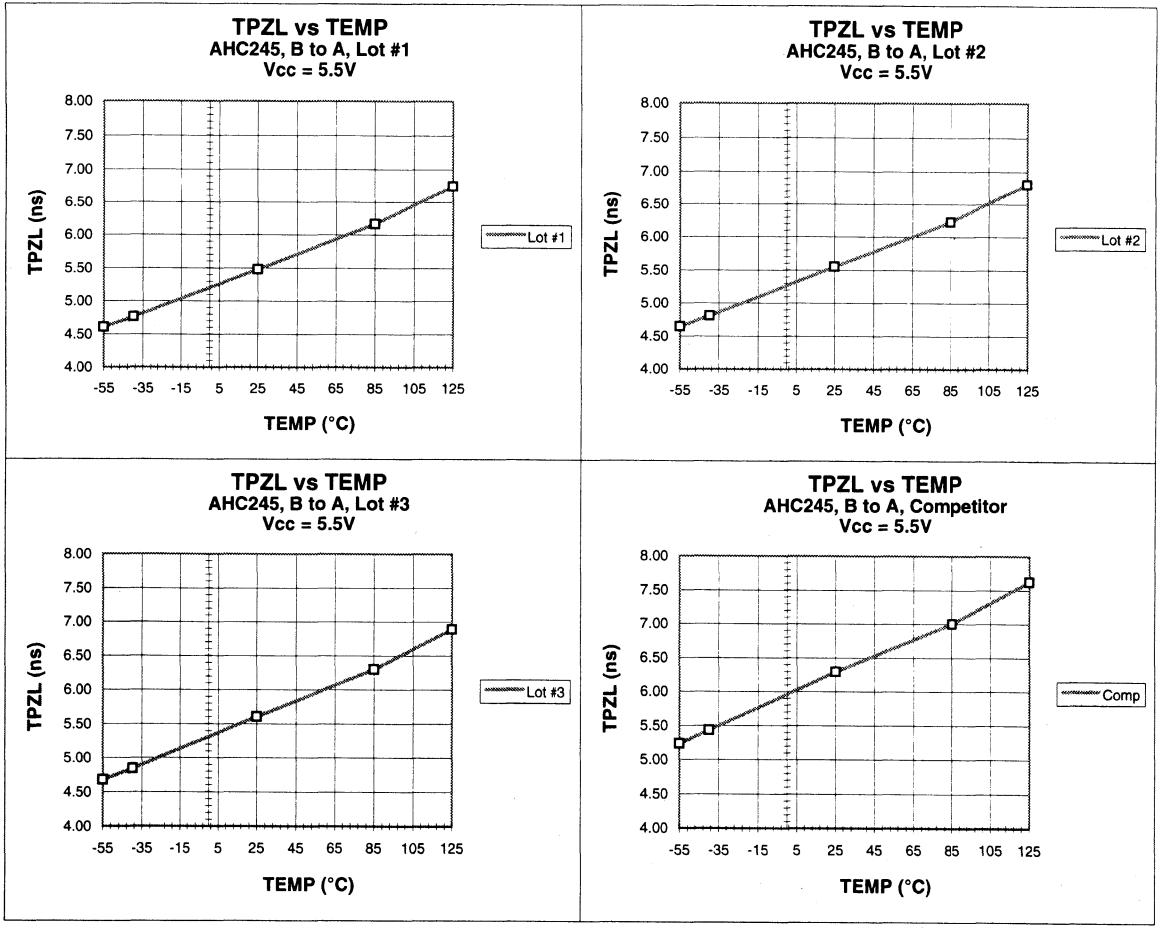

TPZH vs TEMP
AHC245, B to A, Lot #1
Vcc = 3.0V
TPZH (ns)
11.50
11.00
10.50
10.00
9.50
9.00
8.50
8.00
7.50
7.00
6.50
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Lot #1
TPZH vs TEMP
AHC245, B to A, Lot #2
Vcc = 3.0V
TPZH (ns)
11.50
11.00
10.50
10.00
9.50
9.00
8.50
8.00
7.50
7.00
6.50
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Lot #2
TPZH vs TEMP
AHC245, B to A, Lot #3
Vcc = 3.0V
TPZH (ns)
11.50
11.00
10.50
10.00
9.50
9.00
8.50
8.00
7.50
7.00
6.50
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Lot #3
TPZH vs TEMP
AHC245, B to A, Competitor
Vcc = 3.0V
TPZH (ns)
11.50
10.50
9.50
8.50
7.50
6.50
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Comp

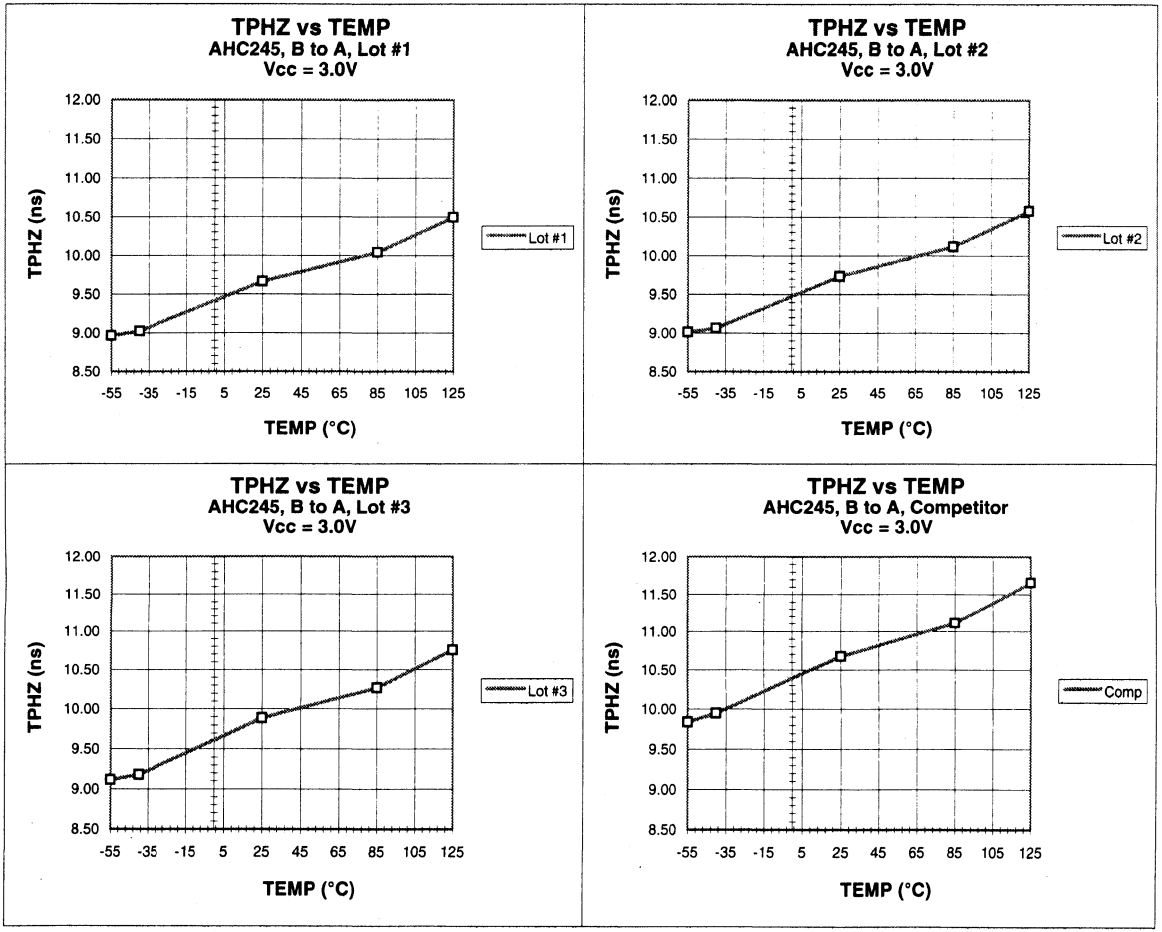

TPZH vs TEMP
AHC245, B to A, Lot #1
Vcc = 4.5V
TPZH (ns)
8.50
8.00
7.50
7.00
6.50
6.00
5.50
5.00
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Lot #1
TPZH vs TEMP
AHC245, B to A, Lot #2
Vcc = 4.5V
TPZH (ns)
8.50
8.00
7.50
7.00
6.50
6.00
5.50
5.00
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Lot #2
TPZH vs TEMP
AHC245, B to A, Lot #3
Vcc = 4.5V
TPZH (ns)
8.50
8.00
7.50
7.00
6.50
6.00
5.50
5.00
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Lot #3
TPZH vs TEMP
AHC245, B to A, Competitor
Vcc = 4.5V
TPZH (ns)
8.50
8.00
7.50
7.00
6.50
6.00
5.50
5.00
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Comp

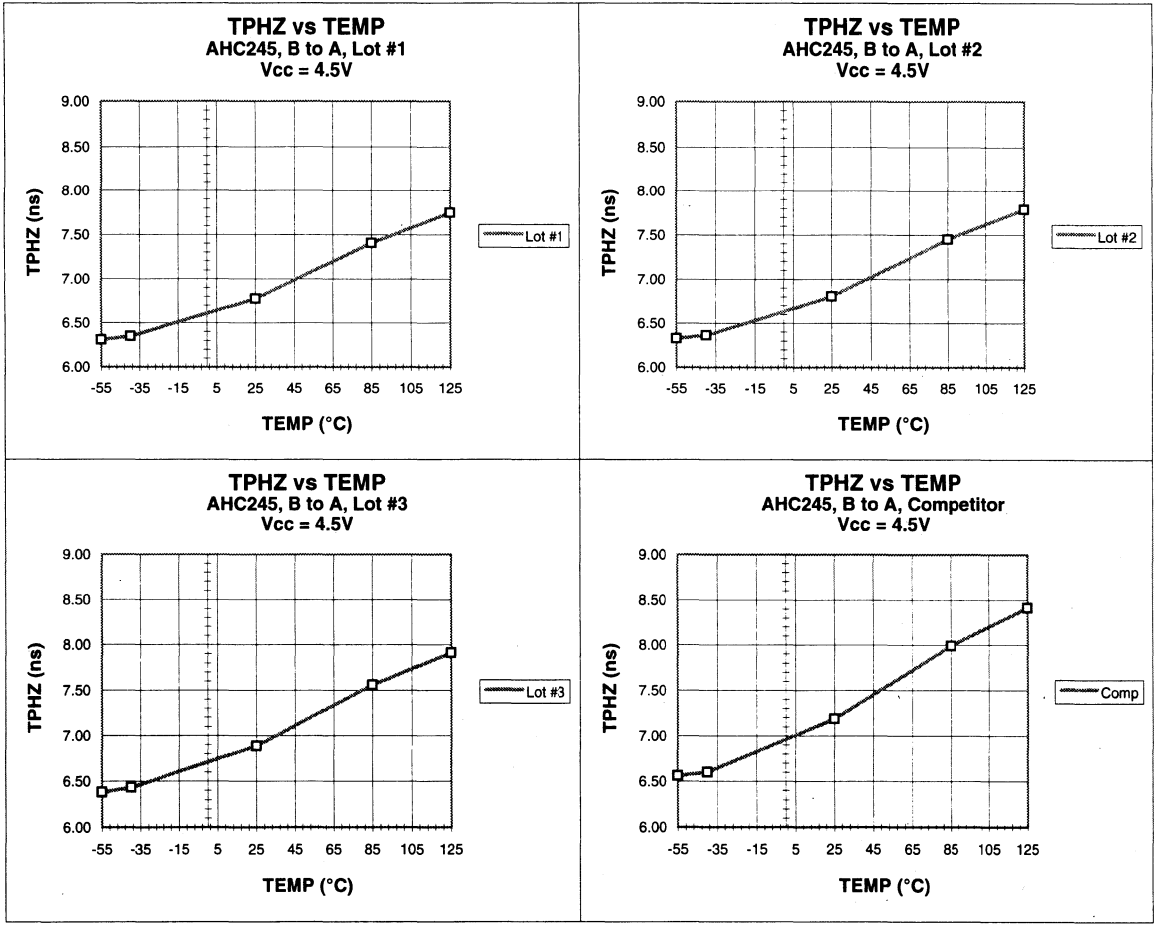

TPZH vs TEMP
AHC245, B to A, Lot #1
Vcc = 5.5V
TPZH (ns)
7.50
7.00
6.50
6.00
5.50
5.00
4.50
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Lot #1
TPZH vs TEMP
AHC245, B to A, Lot #2
Vcc = 5.5V
TPZH (ns)
7.50
7.00
6.50
6.00
5.50
5.00
4.50
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Lot #2
TPZH vs TEMP
AHC245, B to A, Lot #3
Vcc = 5.5V
TPZH (ns)
7.50
7.00
6.50
6.00
5.50
5.00
4.50
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Lot #3
TPZH vs TEMP
AHC245, B to A, Competitor
Vcc = 5.5V
TPZH (ns)
7.50
7.00
6.50
6.00
5.50
5.00
4.50
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Comp

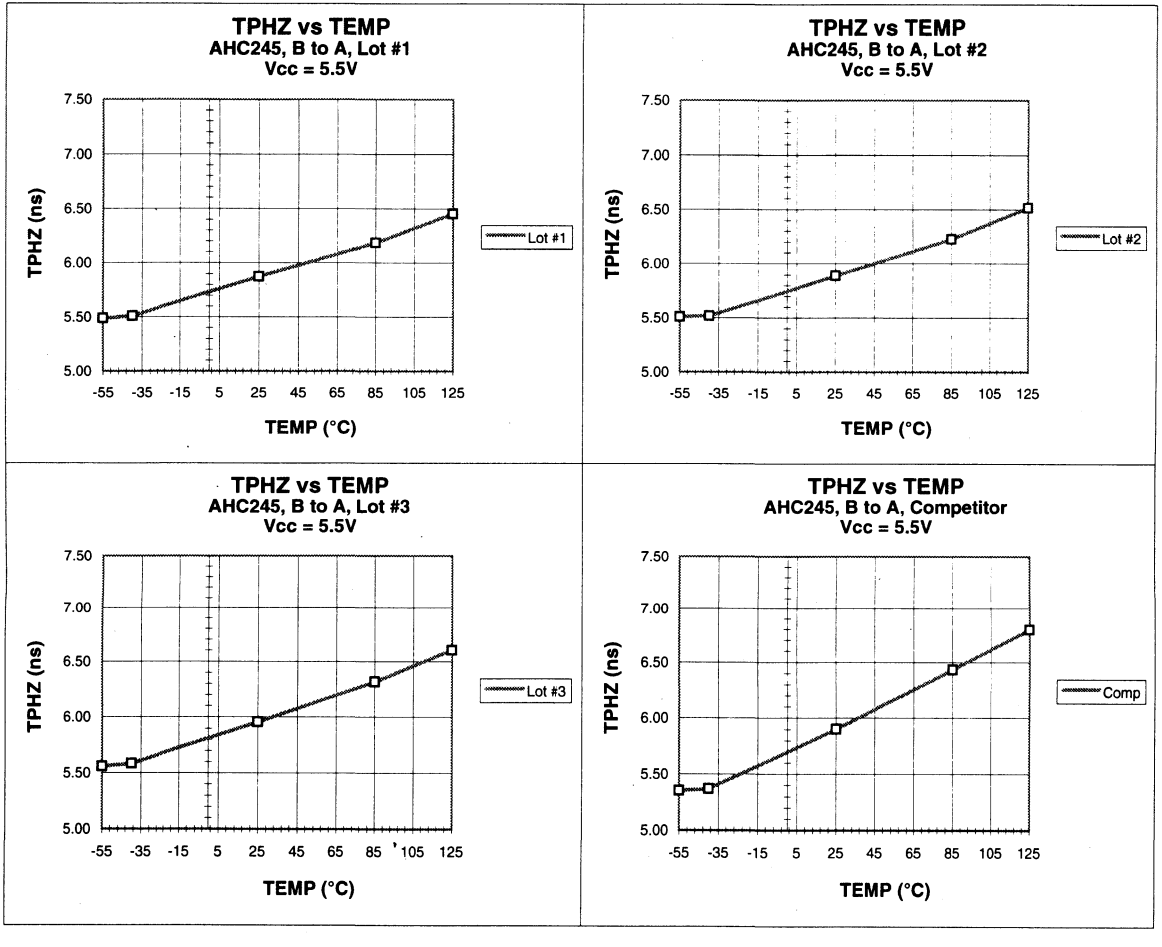

TPZL vs TEMP
AHC245, B to A, Lot #1
Vcc = 3.0V
TPZL (ns)
14.00
13.00
12.00
11.00
10.00
9.00
8.00
7.00
6.00
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Lot #1
TPZL vs TEMP
AHC245, B to A, Lot #2
Vcc = 3.0V
TPZL (ns)
14.00
13.00
12.00
11.00
10.00
9.00
8.00
7.00
6.00
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Lot #2
TPZL vs TEMP
AHC245, B to A, Lot #3
Vcc = 3.0V
TPZL (ns)
14.00
13.00
12.00
11.00
10.00
9.00
8.00
7.00
6.00
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Lot #3
TPZL vs TEMP
AHC245, B to A, Competitor
Vcc = 3.0V
TPZL (ns)
14.00
13.00
12.00
11.00
10.00
9.00
8.00
7.00
6.00
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Comp

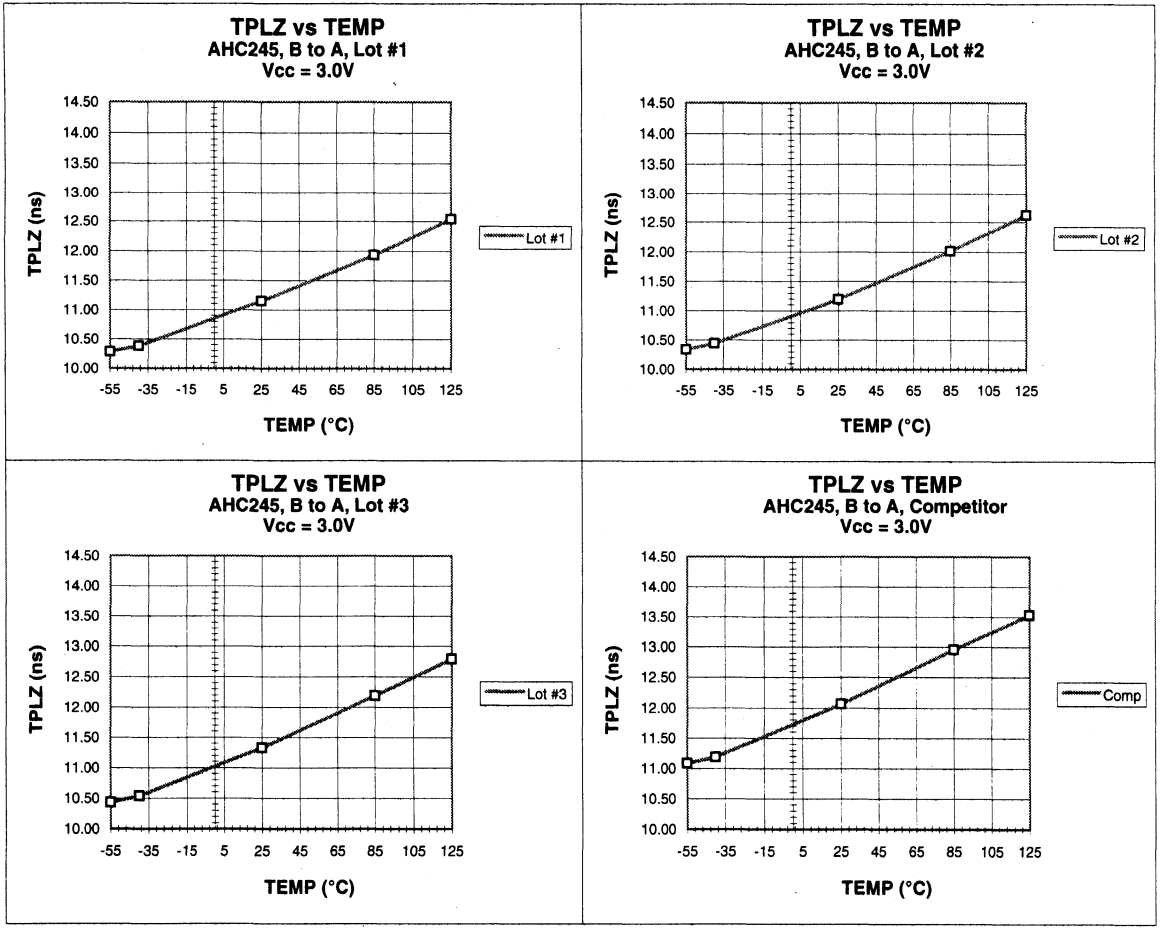

TPZL vs TEMP
AHC245, B to A, Lot #1
Vcc = 4.5V
TPZL (ns)
9.50
9.00
8.50
8.00
7.50
7.00
6.50
6.00
5.50
5.00
4.50
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Lot #1
TPZL vs TEMP
AHC245, B to A, Lot #2
Vcc = 4.5V
TPZL (ns)
9.50
9.00
8.50
8.00
7.50
7.00
6.50
6.00
5.50
5.00
4.50
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Lot #2
TPZL vs TEMP
AHC245, B to A, Lot #3
Vcc = 4.5V
TPZL (ns)
9.50
9.00
8.50
8.00
7.50
7.00
6.50
6.00
5.50
5.00
4.50
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Lot #3
TPZL vs TEMP
AHC245, B to A, Competitor
Vcc = 4.5V
TPZL (ns)
9.50
9.00
8.50
8.00
7.50
7.00
6.50
6.00
5.50
5.00
4.50
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Comp

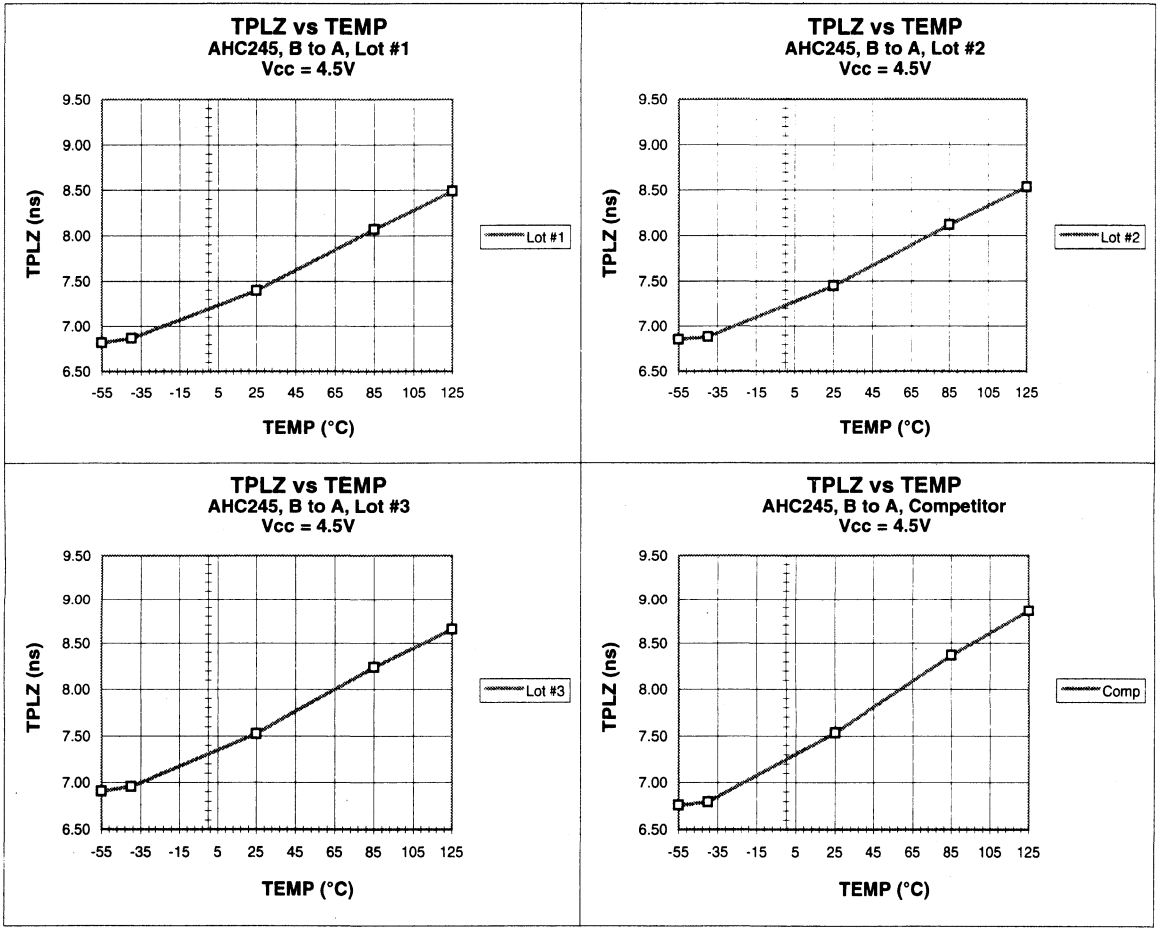

TPZL vs TEMP
AHC245, B to A, Lot #1
Vcc = 5.5V
TPZL (ns)
8.00
7.50
7.00
6.50
6.00
5.50
5.00
4.50
4.00
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Lot #1
TPZL vs TEMP
AHC245, B to A, Lot #2
Vcc = 5.5V
TPZL (ns)
8.00
7.50
7.00
6.50
6.00
5.50
5.00
4.50
4.00
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Lot #2
TPZL vs TEMP
AHC245, B to A, Lot #3
Vcc = 5.5V
TPZL (ns)
8.00
7.50
7.00
6.50
6.00
5.50
5.00
4.50
4.00
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Lot #3
TPZL vs TEMP
AHC245, B to A, Competitor
Vcc = 5.5V
TPZL (ns)
8.00
7.50
7.00
6.50
6.00
5.50
5.00
4.50
4.00
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Comp

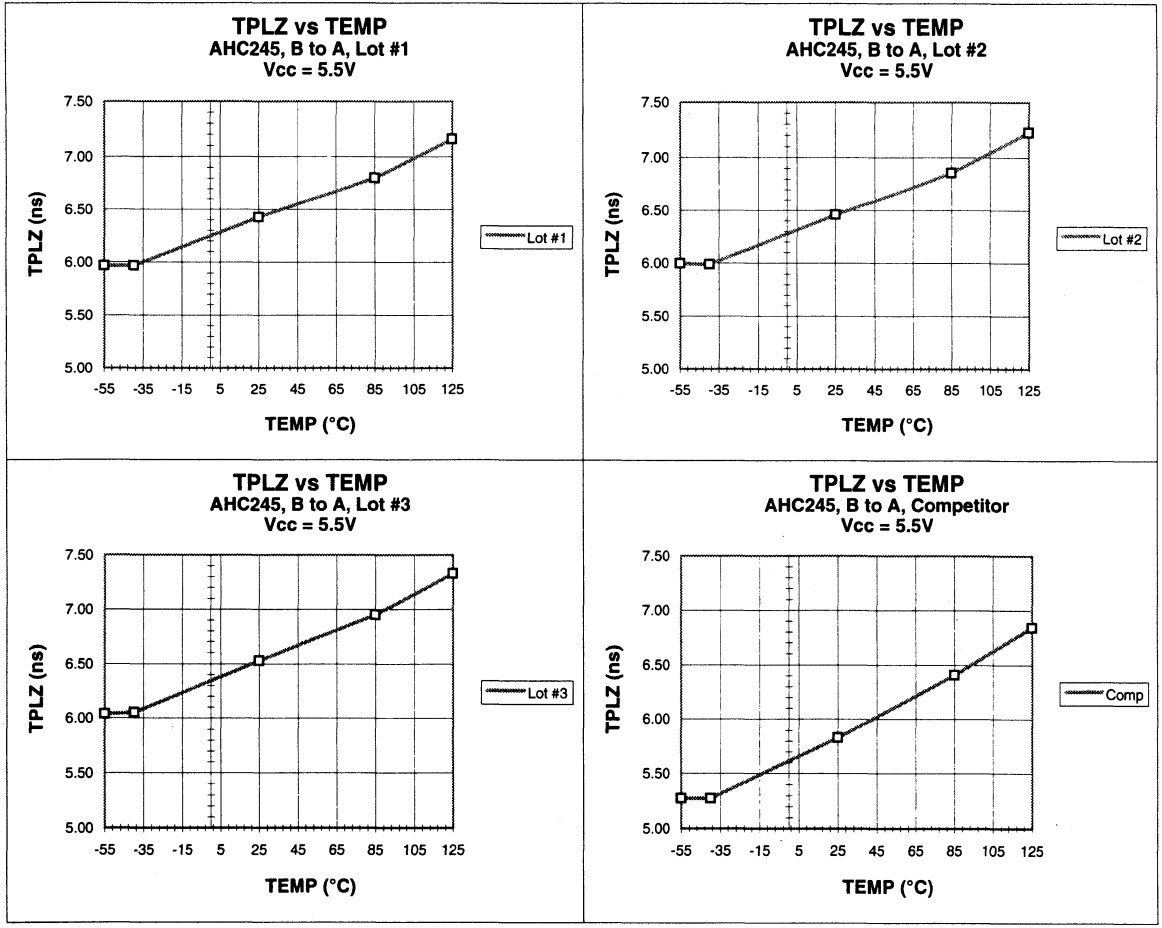

TPHZ vs TEMP
AHC245, B to A, Lot #1
Vcc = 3.0V
TPHZ (ns)
12.00
11.50
11.00
10.50
10.00
9.50
9.00
8.50
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Lot #1
TPHZ vs TEMP
AHC245, B to A, Lot #2
Vcc = 3.0V
TPHZ (ns)
12.00
11.50
11.00
10.50
10.00
9.50
9.00
8.50
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Lot #2
TPHZ vs TEMP
AHC245, B to A, Lot #3
Vcc = 3.0V
TPHZ (ns)
12.00
11.50
11.00
10.50
10.00
9.50
9.00
8.50
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Lot #3
TPHZ vs TEMP
AHC245, B to A, Competitor
Vcc = 3.0V
TPHZ (ns)
12.00
11.50
11.00
10.50
10.00
9.50
9.00
8.50
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Comp


TPHZ vs TEMP
AHC245, B to A, Lot #1
Vcc = 4.5V
TPHZ (ns)
9.00
8.50
8.00
7.50
7.00
6.50
6.00
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Lot #1
TPHZ vs TEMP
AHC245, B to A, Lot #2
Vcc = 4.5V
TPHZ (ns)
9.00
8.50
8.00
7.50
7.00
6.50
6.00
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Lot #2
TPHZ vs TEMP
AHC245, B to A, Lot #3
Vcc = 4.5V
TPHZ (ns)
9.00
8.50
8.00
7.50
7.00
6.50
6.00
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Lot #3
TPHZ vs TEMP
AHC245, B to A, Competitor
Vcc = 4.5V
TPHZ (ns)
9.00
8.50
8.00
7.50
7.00
6.50
6.00
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Comp


TPHZ vs TEMP
AHC245, B to A, Lot #1
Vcc = 5.5V
TPHZ (ns)
7.50
7.00
6.50
6.00
5.50
5.00
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Lot #1
TPHZ vs TEMP
AHC245, B to A, Lot #2
Vcc = 5.5V
TPHZ (ns)
7.50
7.00
6.50
6.00
5.50
5.00
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Lot #2
TPHZ vs TEMP
AHC245, B to A, Lot #3
Vcc = 5.5V
TPHZ (ns)
7.50
7.00
6.50
6.00
5.50
5.00
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Lot #3
TPHZ vs TEMP
AHC245, B to A, Competitor
Vcc = 5.5V
TPHZ (ns)
7.50
7.00
6.50
6.00
5.50
5.00
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Comp


TPLZ vs TEMP
AHC245, B to A, Lot #1
Vcc = 3.0V
TPLZ (ns)
14.50
14.00
13.50
13.00
12.50
12.00
11.50
11.00
10.50
10.00
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Lot #1
TPLZ vs TEMP
AHC245, B to A, Lot #2
Vcc = 3.0V
TPLZ (ns)
14.50
14.00
13.50
13.00
12.50
12.00
11.50
11.00
10.50
10.00
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Lot #2
TPLZ vs TEMP
AHC245, B to A, Lot #3
Vcc = 3.0V
TPLZ (ns)
14.50
14.00
13.50
13.00
12.50
12.00
11.50
11.00
10.50
10.00
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Lot #3
TPLZ vs TEMP
AHC245, B to A, Competitor
Vcc = 3.0V
TPLZ (ns)
14.50
14.00
13.50
13.00
12.50
12.00
11.50
11.00
10.50
10.00
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Comp

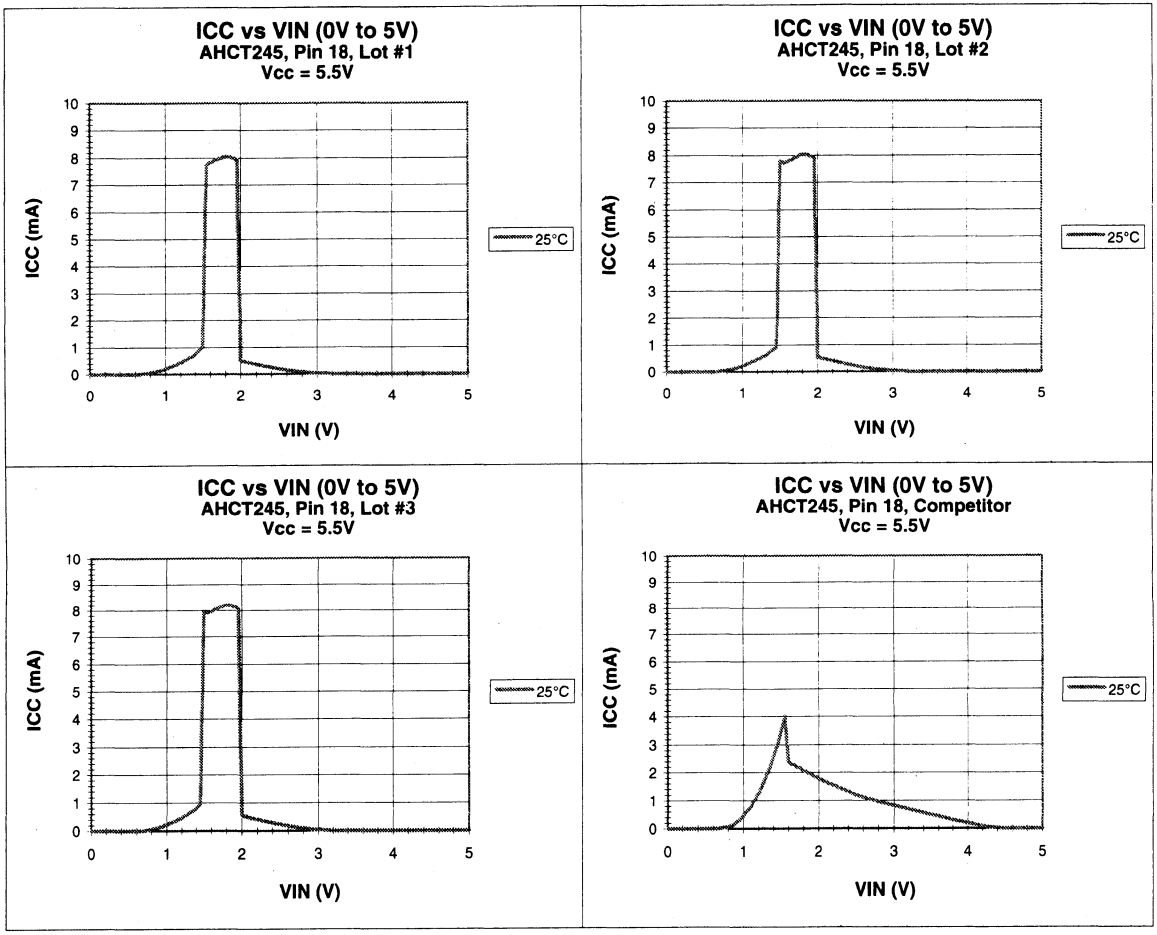

TPLZ vs TEMP
AHC245, B to A, Lot #1
Vcc = 4.5V
TPLZ (ns)
9.50
9.00
8.50
8.00
7.50
7.00
6.50
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Lot #1
TPLZ vs TEMP
AHC245, B to A, Lot #2
Vcc = 4.5V
TPLZ (ns)
9.50
9.00
8.50
8.00
7.50
7.00
6.50
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Lot #2
TPLZ vs TEMP
AHC245, B to A, Lot #3
Vcc = 4.5V
TPLZ (ns)
9.50
9.00
8.50
8.00
7.50
7.00
6.50
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Lot #3
TPLZ vs TEMP
AHC245, B to A, Competitor
Vcc = 4.5V
TPLZ (ns)
9.50
9.00
8.50
8.00
7.50
7.00
6.50
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Comp

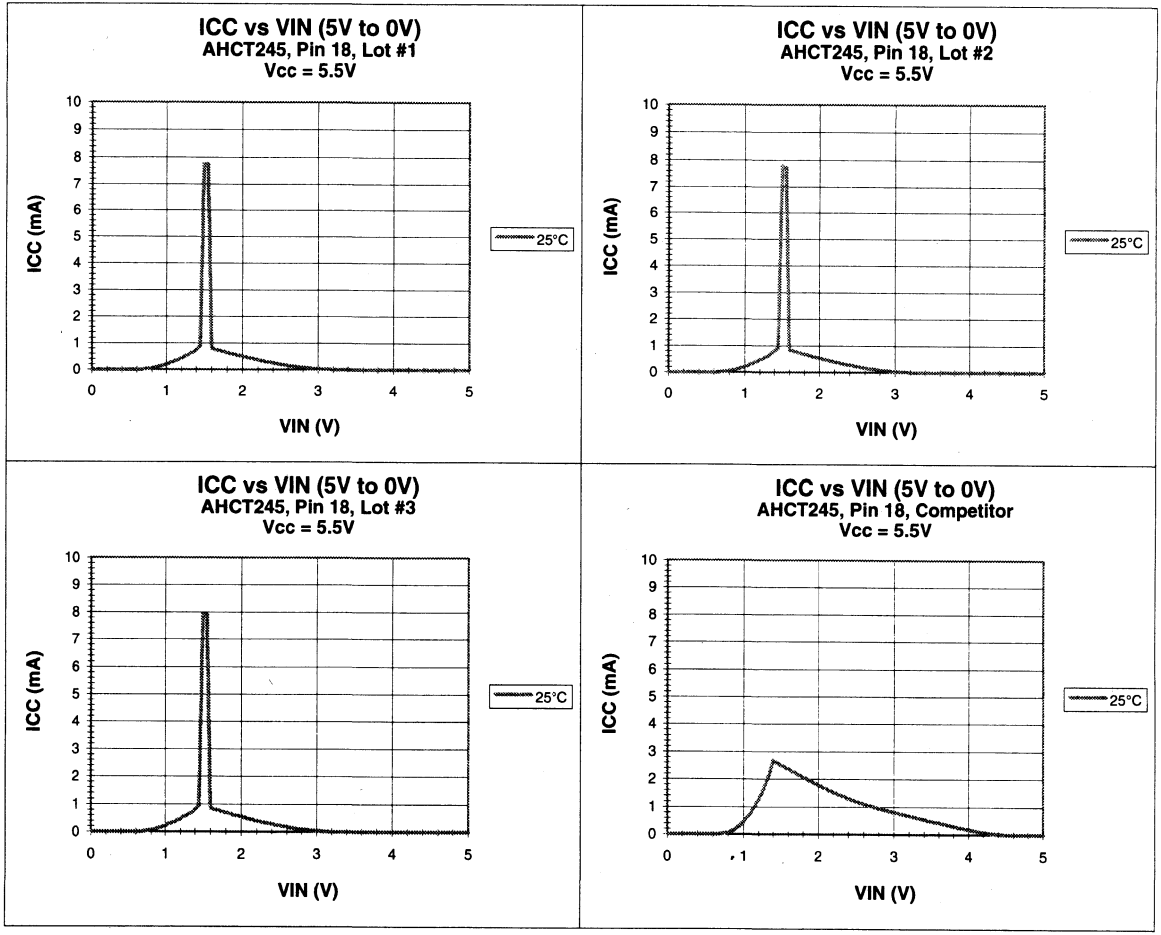

TPLZ vs TEMP
AHC245, B to A, Lot #1
Vcc = 5.5V
TPLZ (ns)
7.50
7.00
6.50
6.00
5.50
5.00
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Lot #1
TPLZ vs TEMP
AHC245, B to A, Lot #2
Vcc = 5.5V
TPLZ (ns)
7.50
7.00
6.50
6.00
5.50
5.00
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Lot #2
TPLZ vs TEMP
AHC245, B to A, Lot #3
Vcc = 5.5V
TPLZ (ns)
7.50
7.00
6.50
6.00
5.50
5.00
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Lot #3
TPLZ vs TEMP
AHC245, B to A, Competitor
Vcc = 5.5V
TPLZ (ns)
7.50
7.00
6.50
6.00
5.50
5.00
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Comp

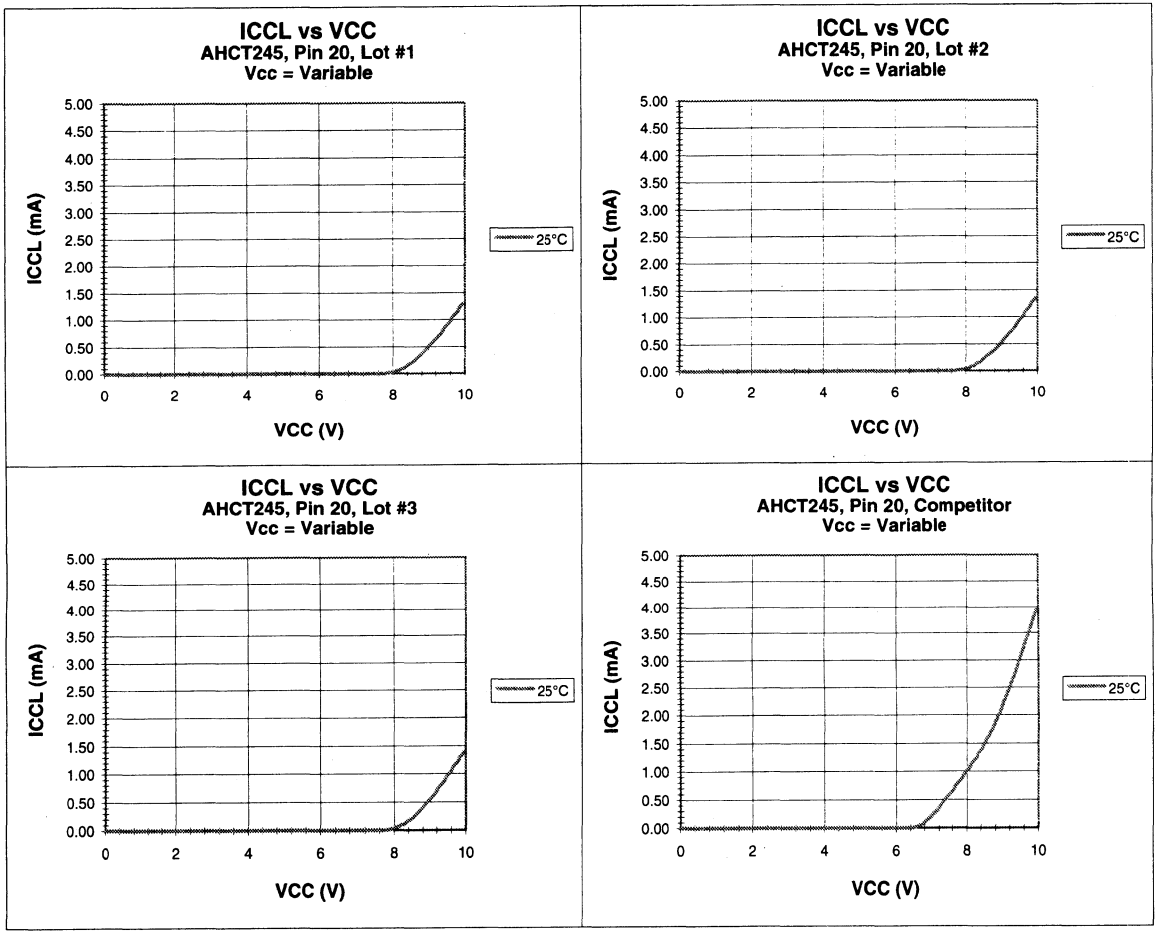
General Information 1
AHC Data Sheets 2
AHCT Data Sheets 3
Mechanical Data 4
AHC04 Qualification Data A
AHCT04 Qualification Data B
AHC245 Qualification Data C
AHCT245 Qualification Data D

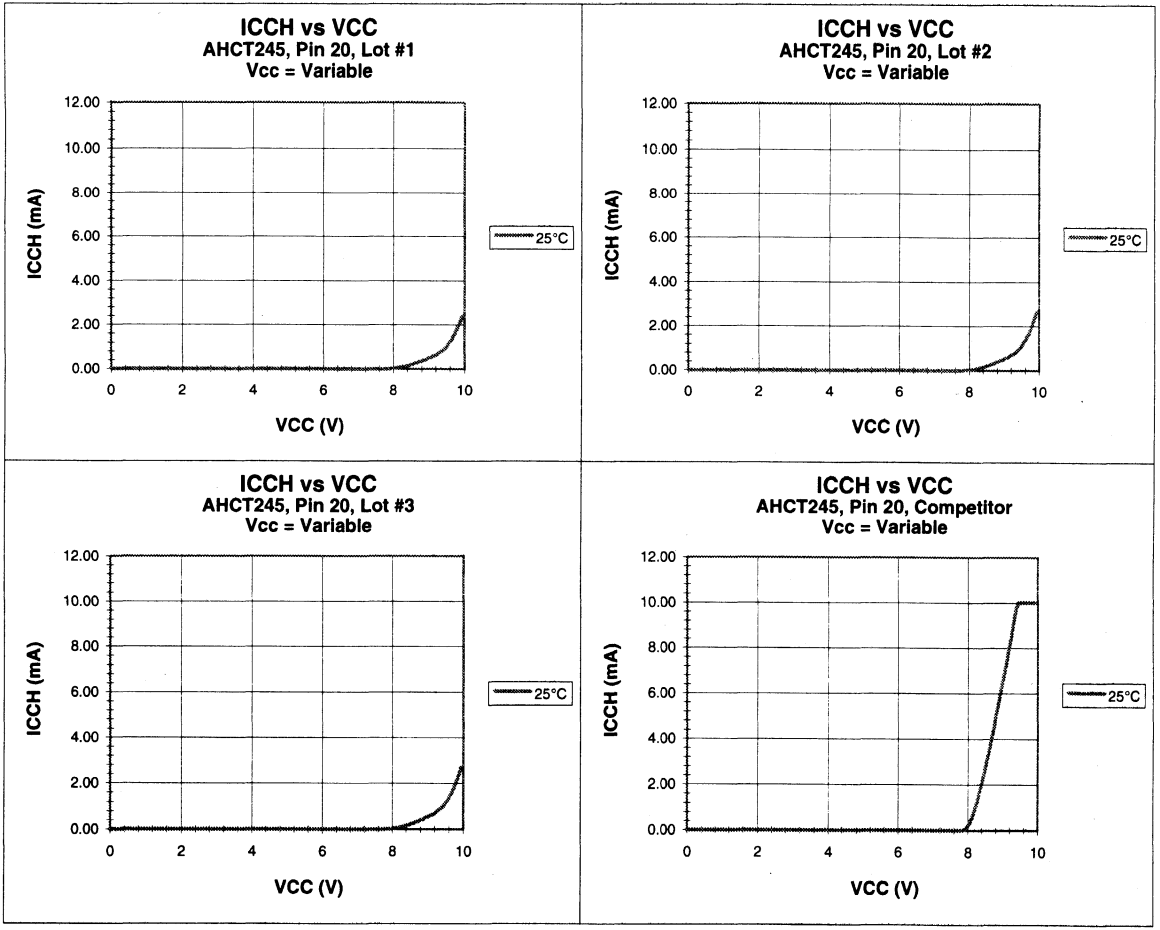
D

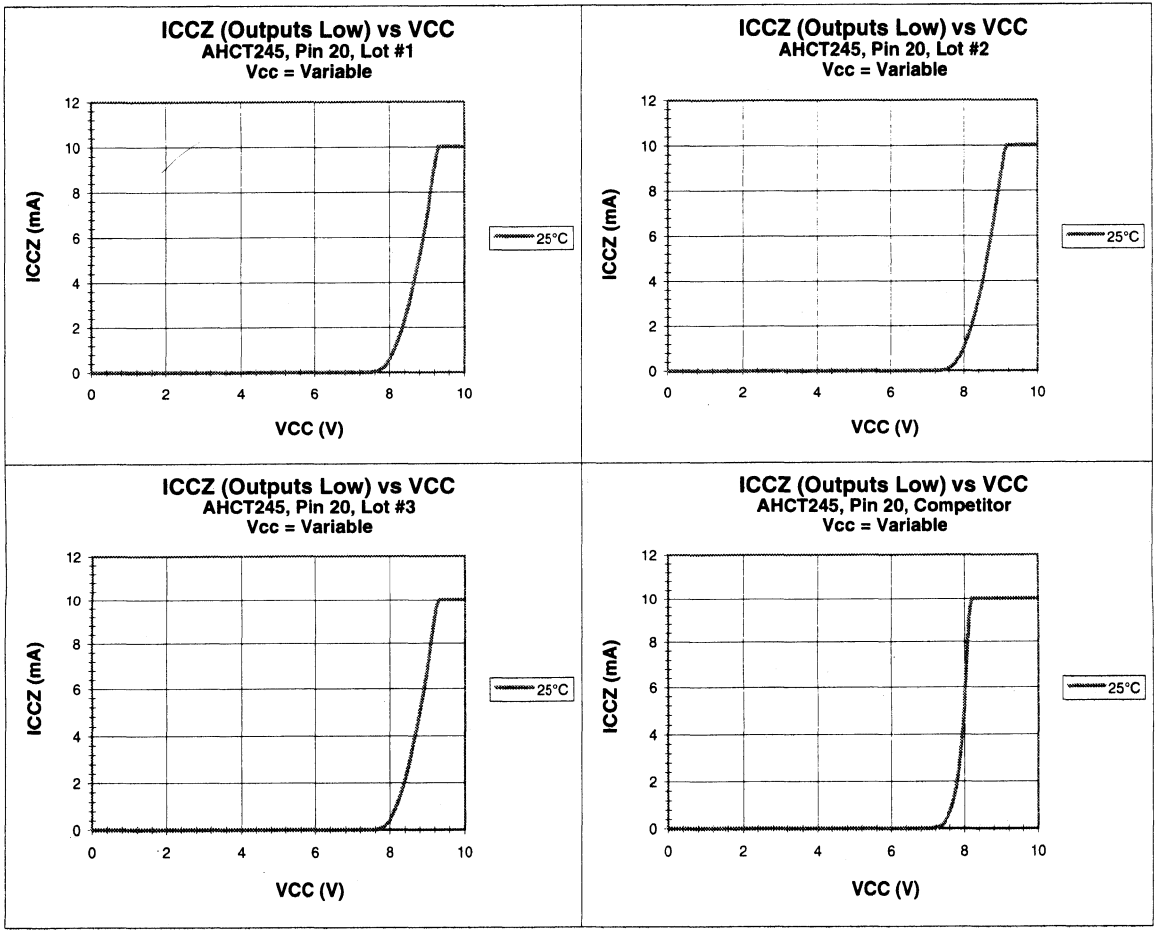
AHCT245 Qualification Data

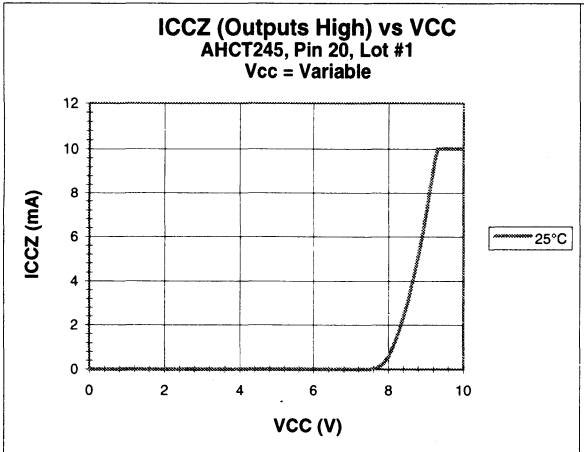

ICC vs VIN (0V to 5V)
AHCT245, Pin 18, Lot #1
Vcc = 5.5V
ICC (mA)
VIN (V)
25°C
ICC vs VIN (0V to 5V)
AHCT245, Pin 18, Lot #2
Vcc = 5.5V
ICC (mA)
VIN (V)
25°C
ICC vs VIN (0V to 5V)
AHCT245, Pin 18, Lot #3
Vcc = 5.5V
ICC (mA)
VIN (V)
25°C
ICC vs VIN (0V to 5V)
AHCT245, Pin 18, Competitor
Vcc = 5.5V
ICC (mA)
VIN (V)
25°C

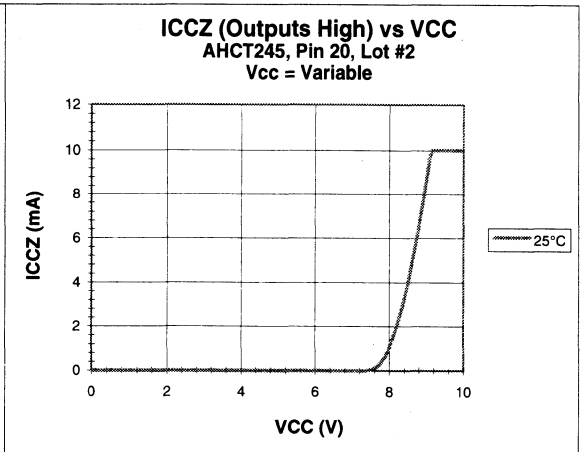

ICC vs VIN (5V to 0V)
AHCT245, Pin 18, Lot #1
Vcc = 5.5V
ICC (mA)
VIN (V)
25°C
ICC vs VIN (5V to 0V)
AHCT245, Pin 18, Lot #2
Vcc = 5.5V
ICC (mA)
VIN (V)
25°C
ICC vs VIN (5V to 0V)
AHCT245, Pin 18, Lot #3
Vcc = 5.5V
ICC (mA)
VIN (V)
25°C
ICC vs VIN (5V to 0V)
AHCT245, Pin 18, Competitor
Vcc = 5.5V
ICC (mA)
VIN (V)
25°C

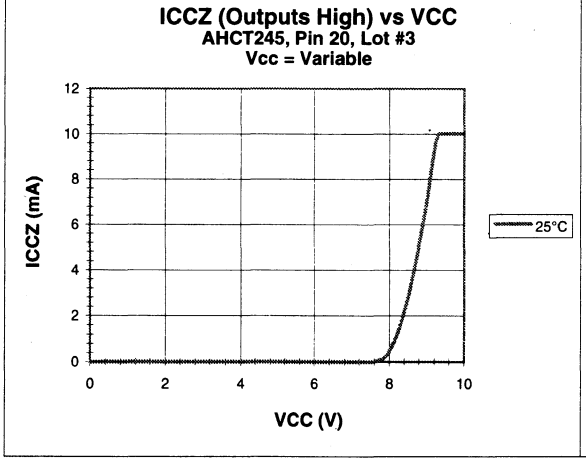

ICCL vs VCC
AHCT245, Pin 20, Lot #1
Vcc = Variable
ICCL (mA)
5.00
4.50
4.00
3.50
3.00
2.50
2.00
1.50
1.00
0.50
0.00
0
2
4
6
8
10
VCC (V)
25°C
ICCL vs VCC
AHCT245, Pin 20, Lot #2
Vcc = Variable
ICCL (mA)
VCC (V)
25°C
ICCL vs VCC
AHCT245, Pin 20, Lot #3
Vcc = Variable
ICCL (mA)
VCC (V)
25°C
ICCL vs VCC
AHCT245, Pin 20, Competitor
Vcc = Variable
ICCL (mA)
VCC (V)
25°C

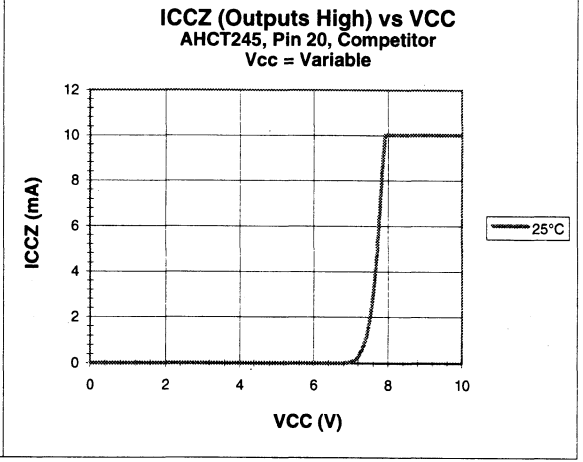

ICCH vs VCC
AHCT245, Pin 20, Lot #1
Vcc = Variable
ICCH (mA)
12.00
10.00
8.00
6.00
4.00
2.00
0.00
0
2
4
6
8
10
VCC (V)
25°C
ICCH vs VCC
AHCT245, Pin 20, Lot #2
Vcc = Variable
ICCH (mA)
VCC (V)
25°C
ICCH vs VCC
AHCT245, Pin 20, Lot #3
Vcc = Variable
ICCH (mA)
VCC (V)
25°C
ICCH vs VCC
AHCT245, Pin 20, Competitor
Vcc = Variable
ICCH (mA)
VCC (V)
25°C

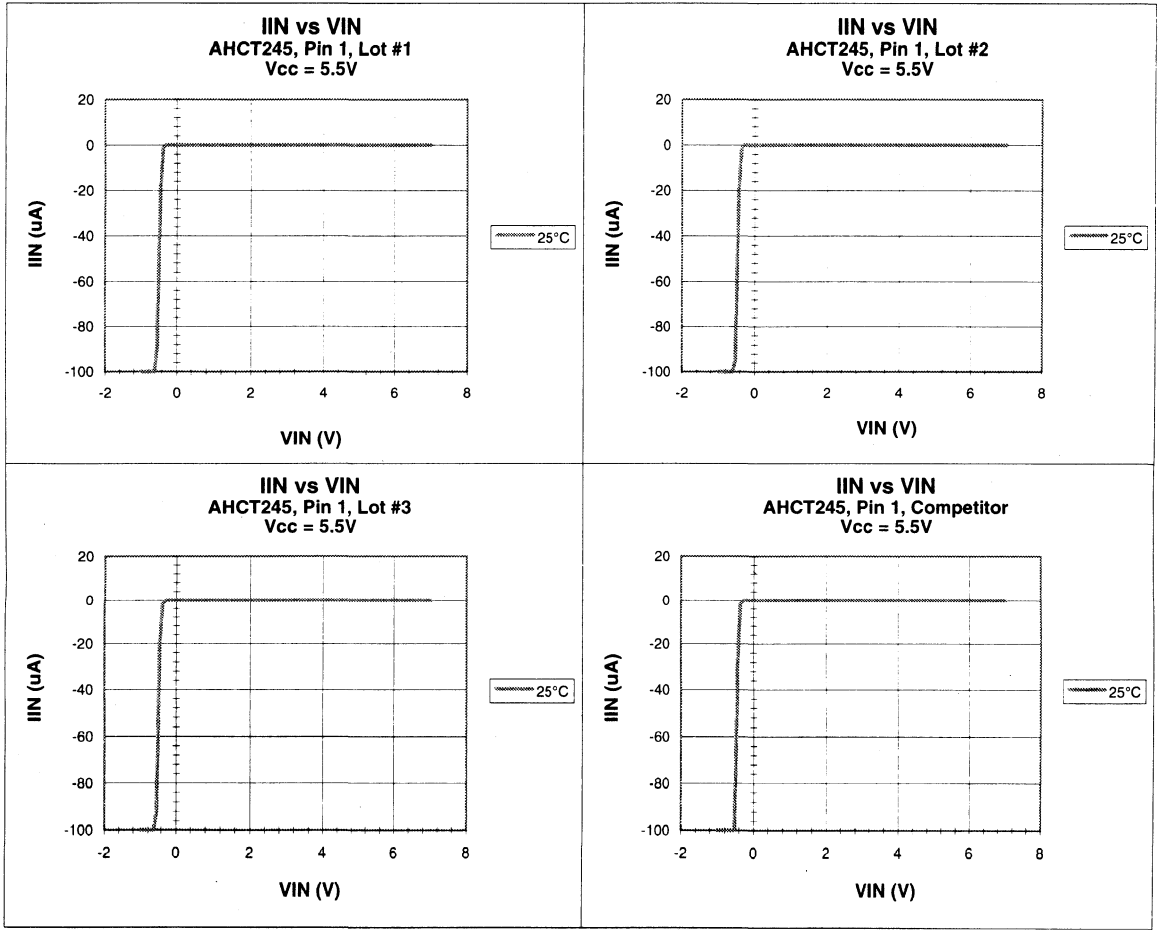

ICCZ (Outputs Low) vs VCC
AHCT245, Pin 20, Lot #1
Vcc = Variable
ICCZ (mA)
VCC (V)
25°C
ICCZ (Outputs Low) vs VCC
AHCT245, Pin 20, Lot #2
Vcc = Variable
ICCZ (mA)
VCC (V)
25°C
ICCZ (Outputs Low) vs VCC
AHCT245, Pin 20, Lot #3
Vcc = Variable
ICCZ (mA)
VCC (V)
25°C
ICCZ (Outputs Low) vs VCC
AHCT245, Pin 20, Competitor
Vcc = Variable
ICCZ (mA)
VCC (V)
25°C

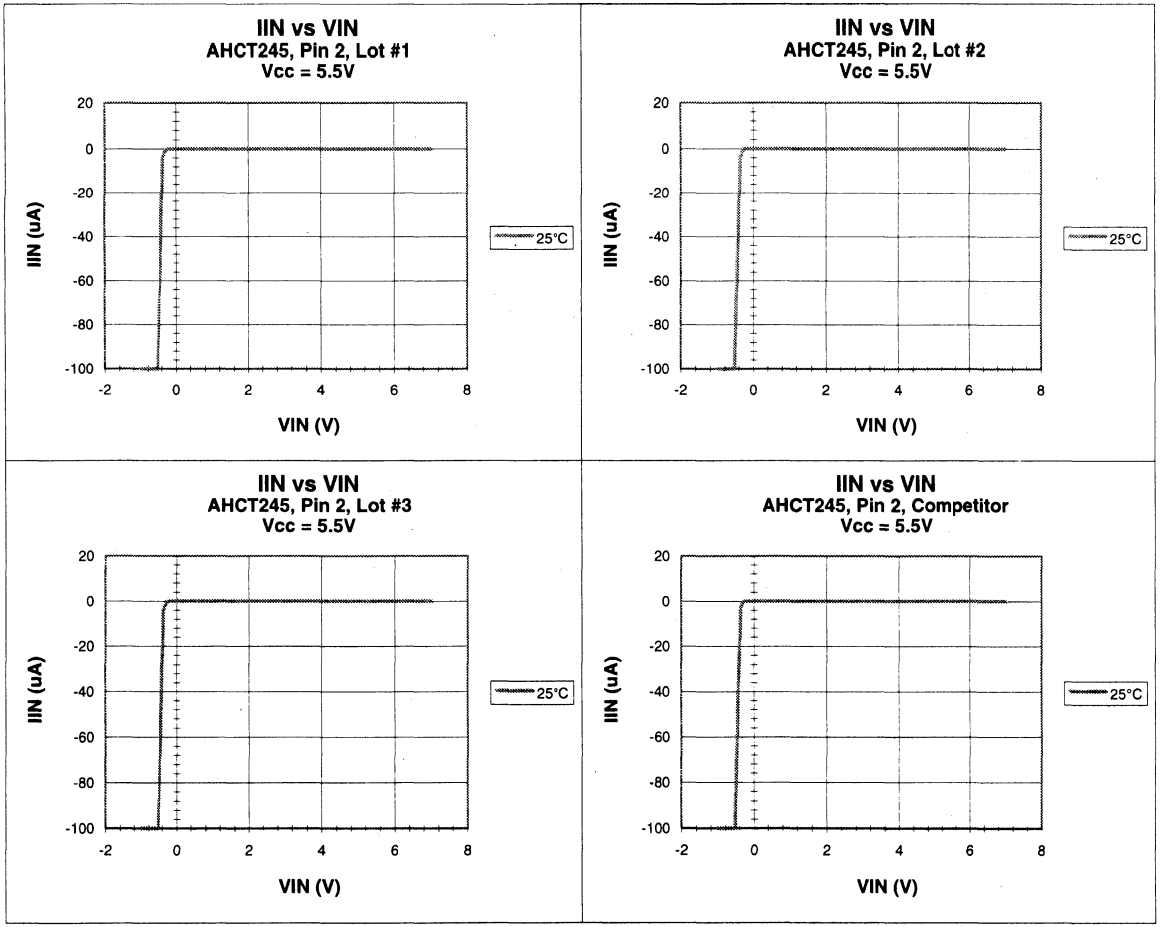

ICCZ (Outputs High) vs VCC
AHCT245, Pin 20, Lot #1
Vcc = Variable
ICCZ (mA)
VCC (V)
25°C

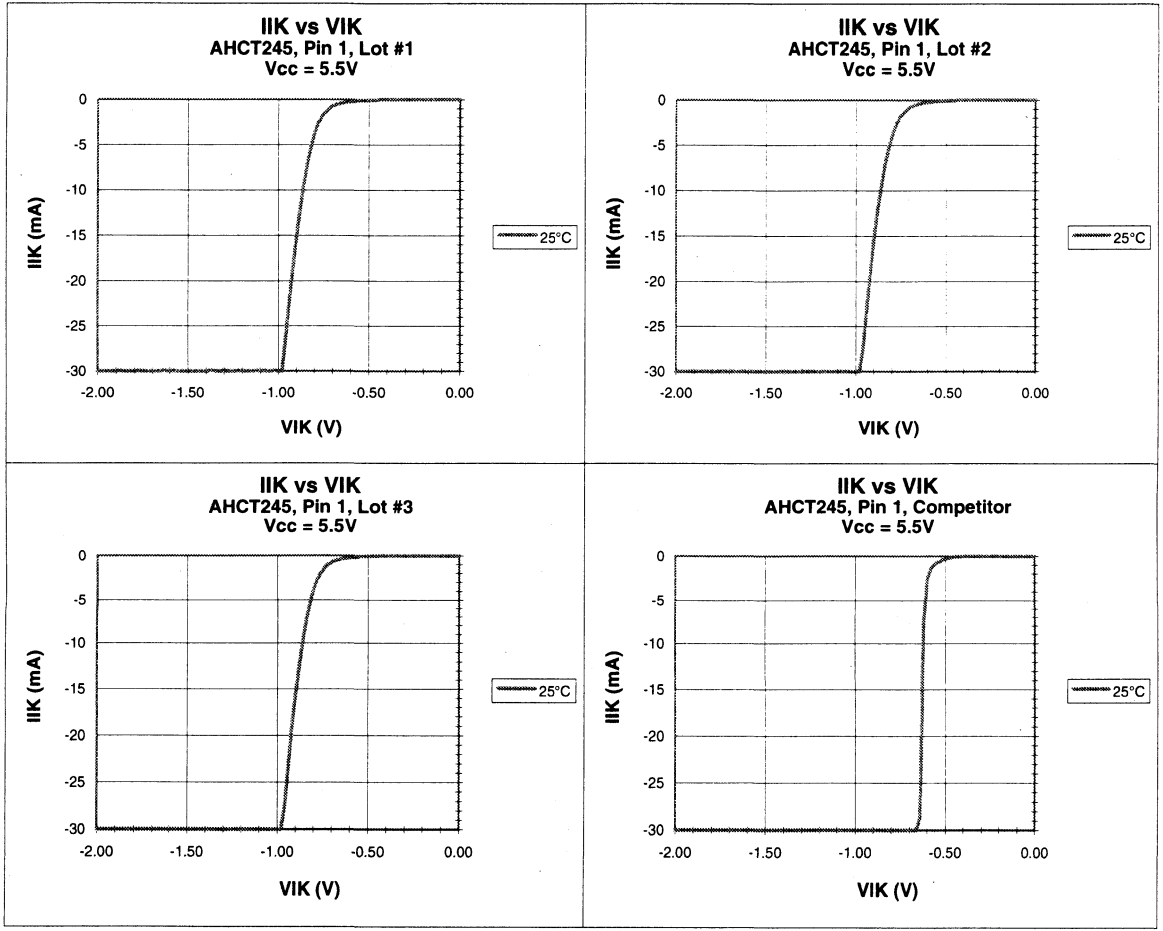

ICCZ (Outputs High) vs VCC
AHCT245, Pin 20, Lot #2
Vcc = Variable
ICCZ (mA)
VCC (V)
25°C

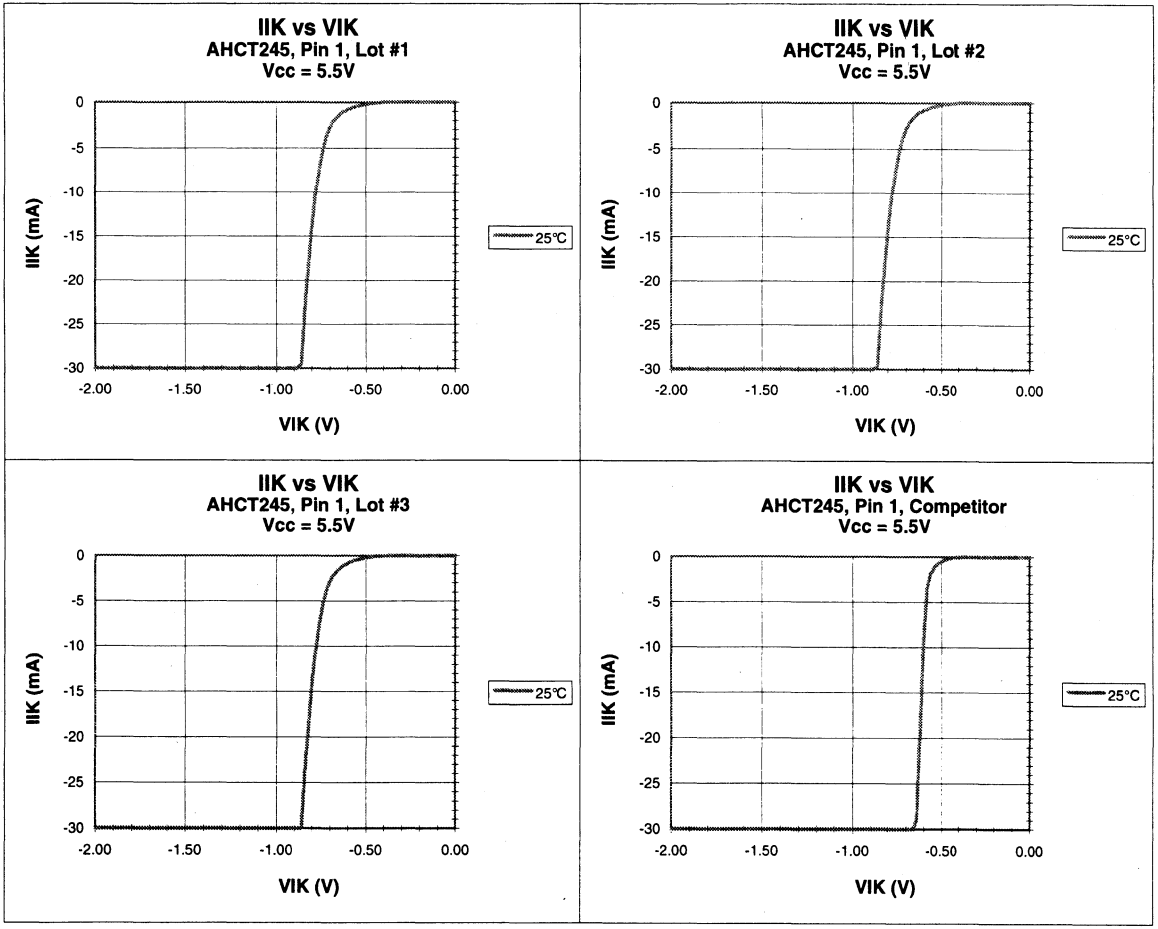

ICCZ (Outputs High) vs VCC
AHCT245, Pin 20, Lot #3
Vcc = Variable
ICCZ (mA)
VCC (V)
25°C

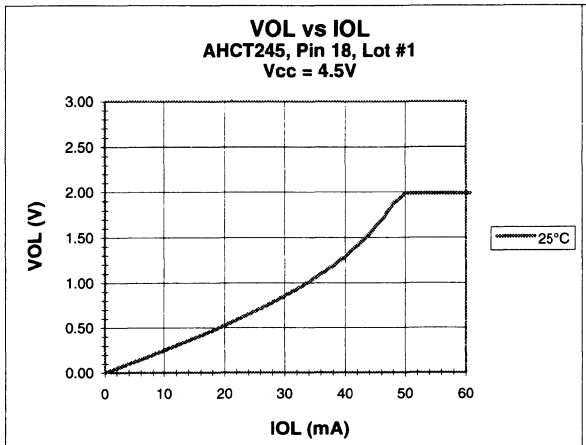

ICCZ (Outputs High) vs VCC
AHCT245, Pin 20, Competitor
Vcc = Variable
ICCZ (mA)
VCC (V)
25°C

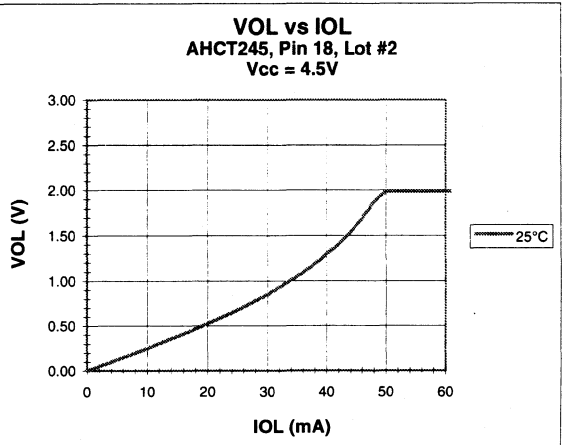

IIN vs VIN
AHCT245, Pin 1, Lot #1
Vcc = 5.5V
IIN (uA)
20
0
-20
-40
-60
-80
-100
-2
0
2
4
6
8
VIN (V)
25°C
IIN vs VIN
AHCT245, Pin 1, Lot #2
Vcc = 5.5V
IIN (uA)
VIN (V)
25°C
IIN vs VIN
AHCT245, Pin 1, Lot #3
Vcc = 5.5V
IIN (uA)
VIN (V)
25°C
IIN vs VIN
AHCT245, Pin 1, Competitor
Vcc = 5.5V
IIN (uA)
VIN (V)
25°C

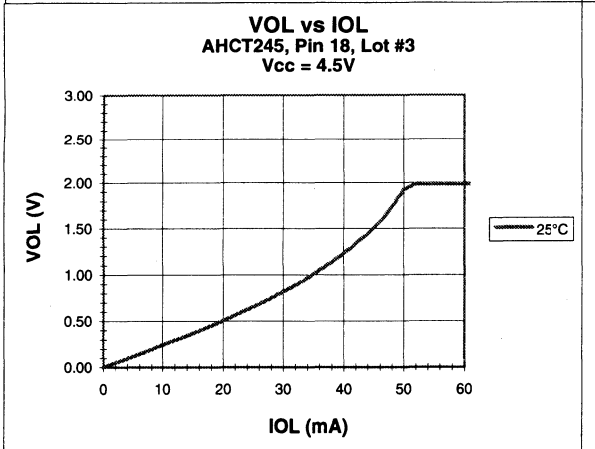

IIN vs VIN
AHCT245, Pin 2, Lot #1
Vcc = 5.5V
IIN (uA)
VIN (V)
25°C
IIN vs VIN
AHCT245, Pin 2, Lot #2
Vcc = 5.5V
IIN (uA)
VIN (V)
25°C
IIN vs VIN
AHCT245, Pin 2, Lot #3
Vcc = 5.5V
IIN (uA)
VIN (V)
25°C
IIN vs VIN
AHCT245, Pin 2, Competitor
Vcc = 5.5V
IIN (uA)
VIN (V)
25°C

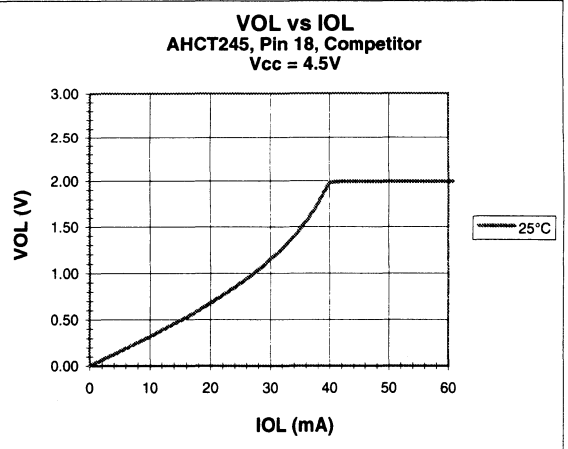

IIK vs VIK
AHCT245, Pin 1, Lot #1
Vcc = 5.5V
IIK (mA)
0
-5
-10
-15
-20
-25
-30
-2.00
-1.50
-1.00
-0.50
0.00
VIK (V)
25°C
IIK vs VIK
AHCT245, Pin 1, Lot #2
Vcc = 5.5V
IIK (mA)
VIK (V)
25°C
IIK vs VIK
AHCT245, Pin 1, Lot #3
Vcc = 5.5V
IIK (mA)
VIK (V)
25°C
IIK vs VIK
AHCT245, Pin 1, Competitor
Vcc = 5.5V
IIK (mA)
VIK (V)
25°C

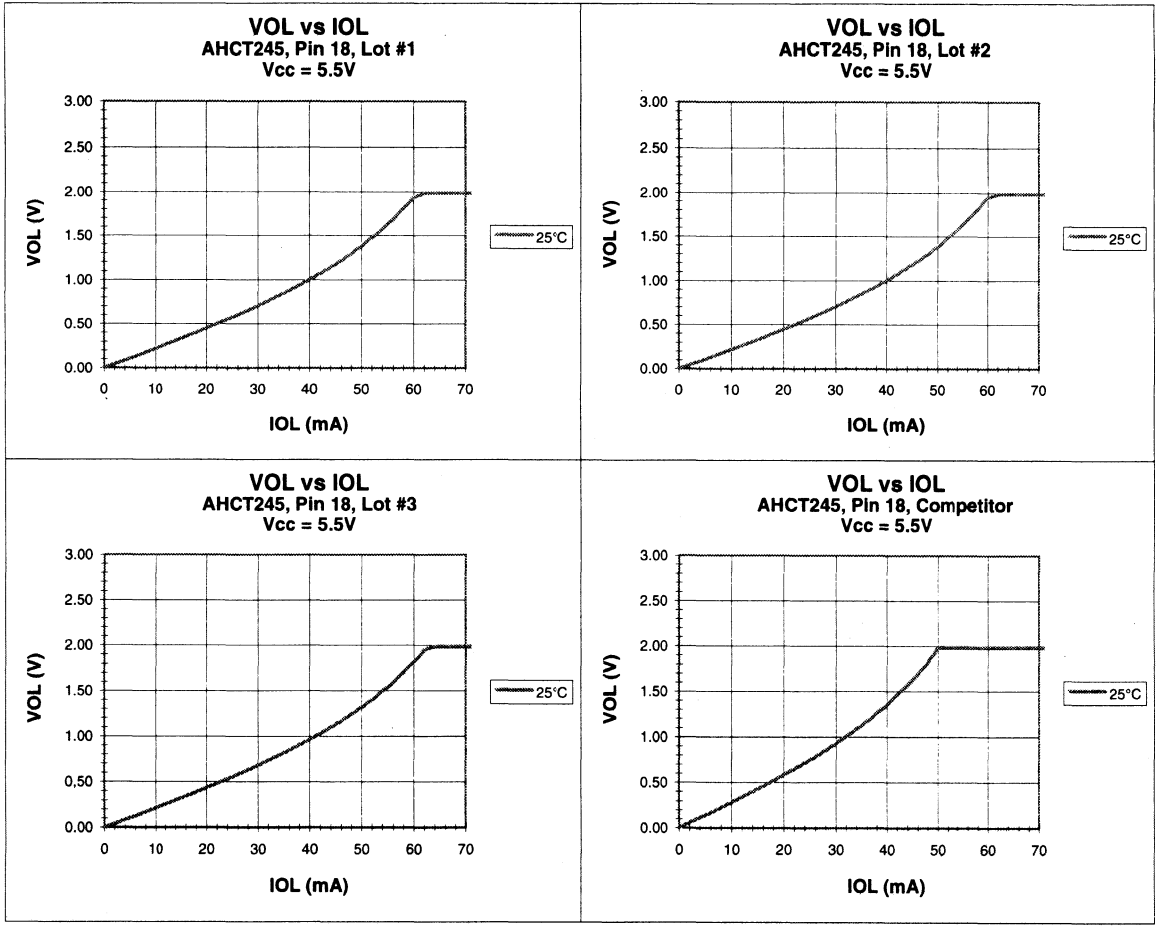

IIK vs VIK
AHCT245, Pin 1, Lot #1
Vcc = 5.5V
IIK (mA)
0
-5
-10
-15
-20
-25
-30
-2.00
-1.50
-1.00
-0.50
0.00
VIK (V)
25°C
IIK vs VIK
AHCT245, Pin 1, Lot #2
Vcc = 5.5V
IIK (mA)
VIK (V)
25°C
IIK vs VIK
AHCT245, Pin 1, Lot #3
Vcc = 5.5V
IIK (mA)
VIK (V)
25°C
IIK vs VIK
AHCT245, Pin 1, Competitor
Vcc = 5.5V
IIK (mA)
VIK (V)
25°C

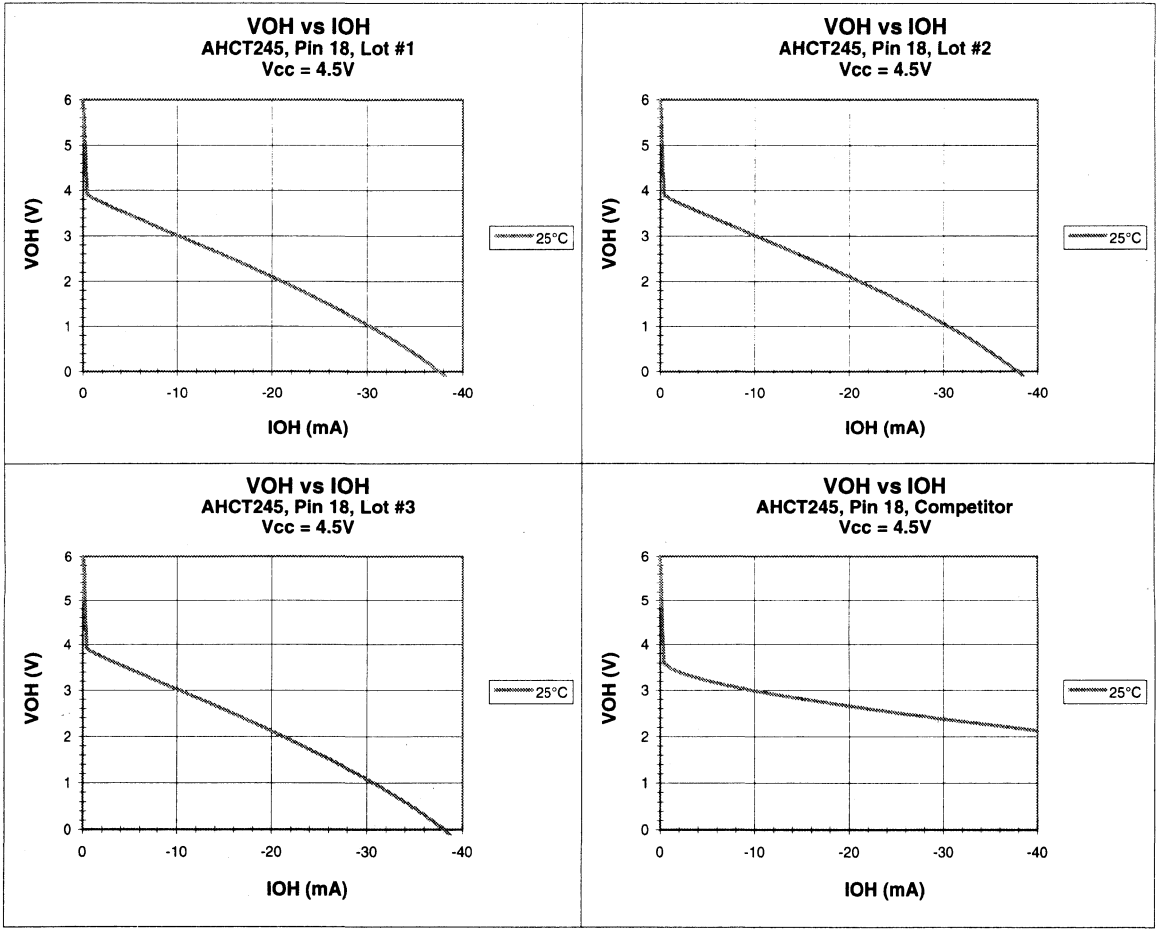

VOL vs IOL
AHCT245, Pin 18, Lot #1
Vcc = 4.5V
VOL (V)
3.00
2.50
2.00
1.50
1.00
0.50
0.00
0
10
20
30
40
50
60
IOL (mA)
25°C

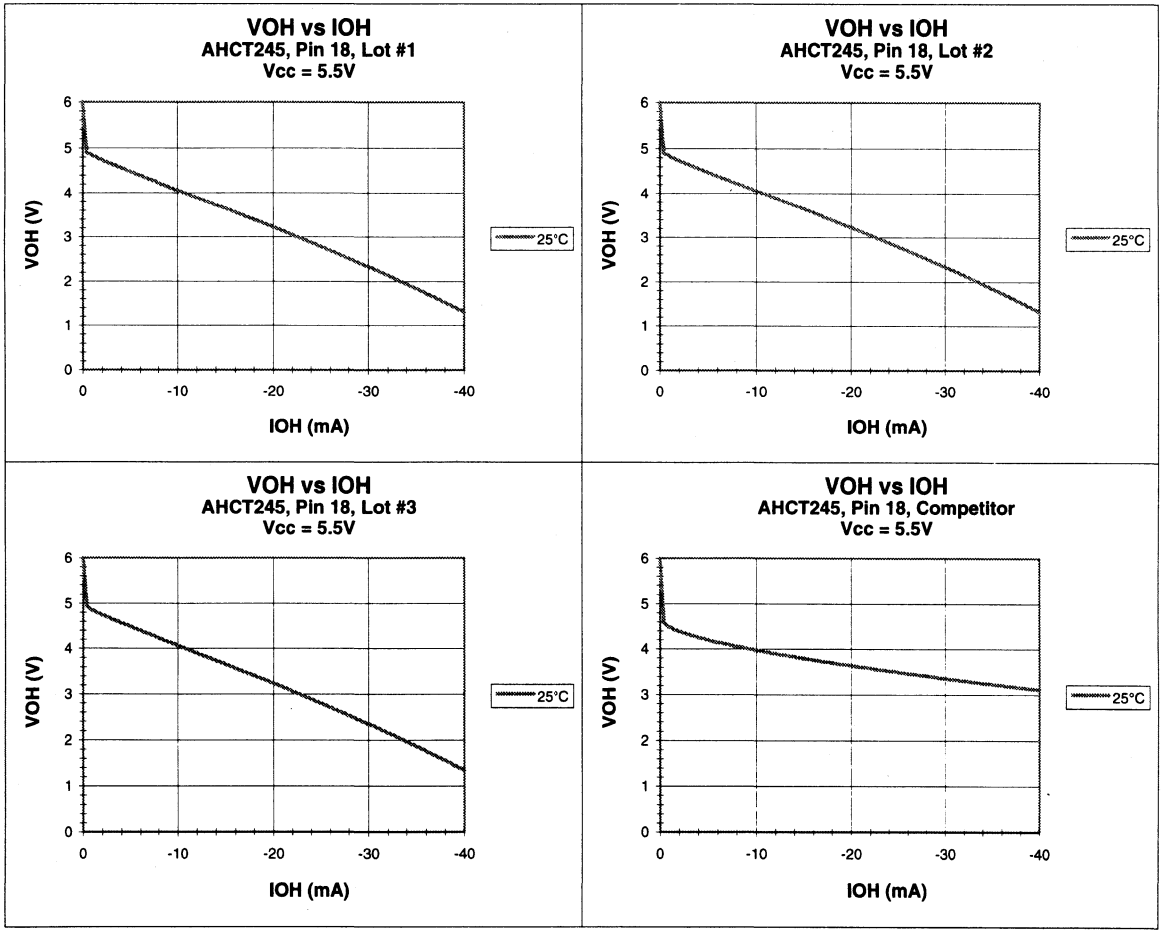

VOL vs IOL
AHCT245, Pin 18, Lot #2
Vcc = 4.5V
VOL (V)
3.00
2.50
2.00
1.50
1.00
0.50
0.00
0
10
20
30
40
50
60
IOL (mA)
25°C

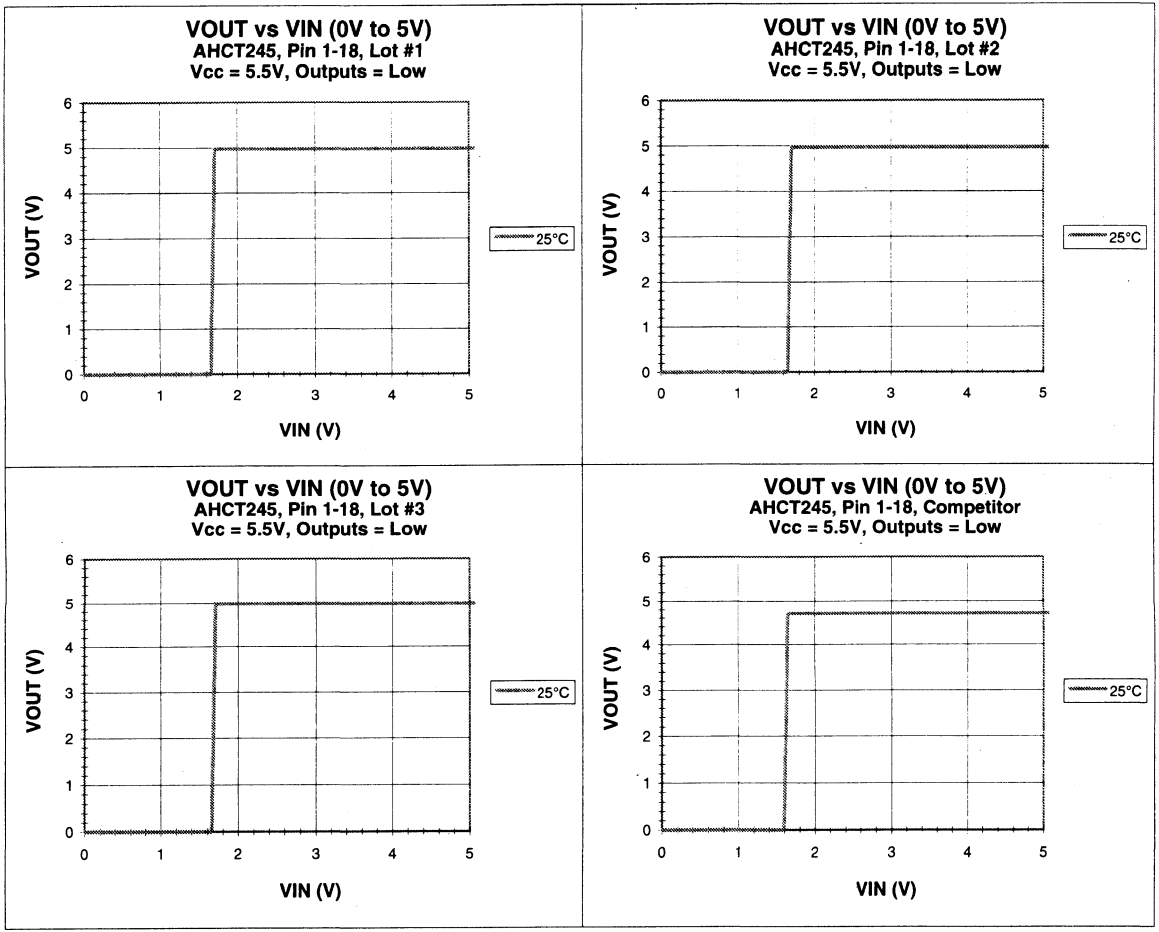

VOL vs IOL
AHCT245, Pin 18, Lot #3
Vcc = 4.5V
VOL (V)
3.00
2.50
2.00
1.50
1.00
0.50
0.00
0
10
20
30
40
50
60
IOL (mA)
25°C

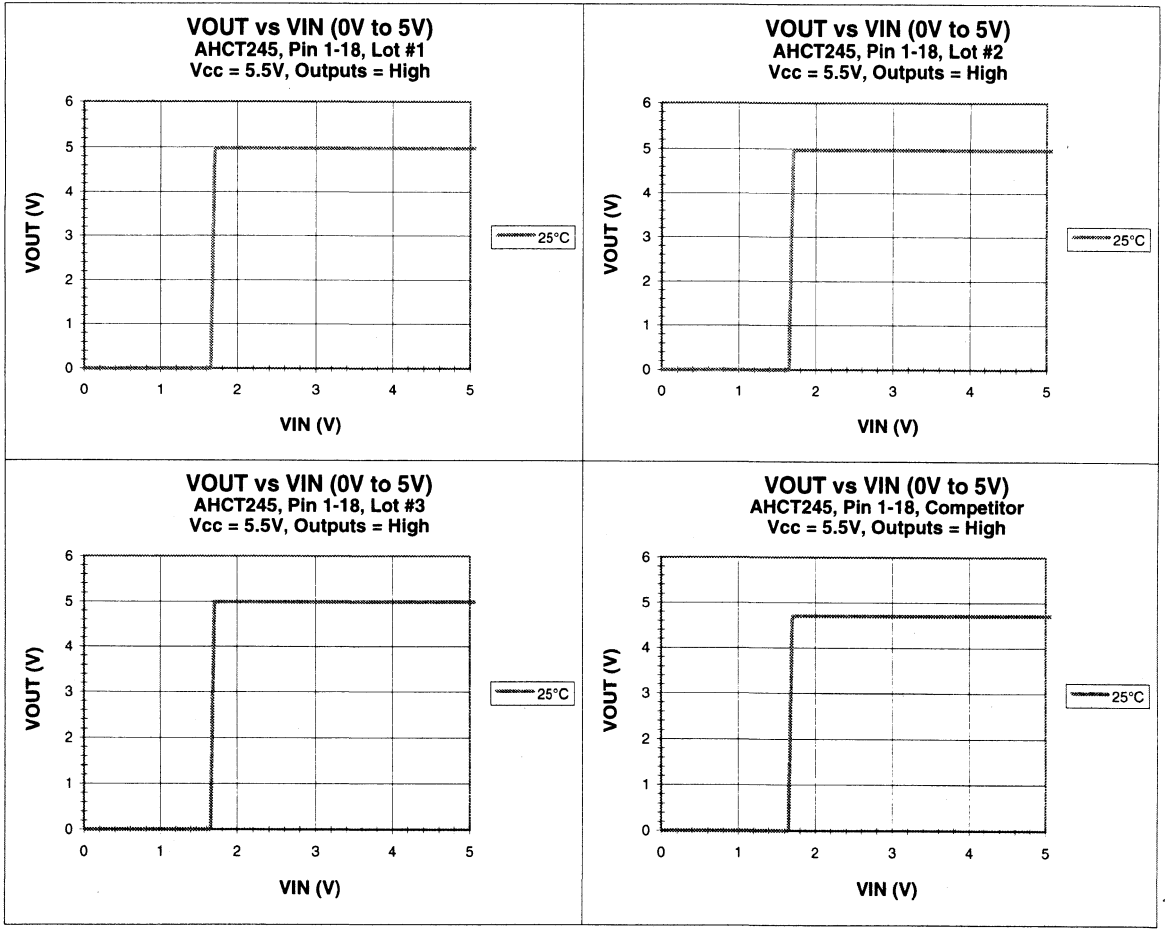

VOL vs IOL
AHCT245, Pin 18, Competitor
Vcc = 4.5V
VOL (V)
3.00
2.50
2.00
1.50
1.00
0.50
0.00
0
10
20
30
40
50
60
IOL (mA)
25°C

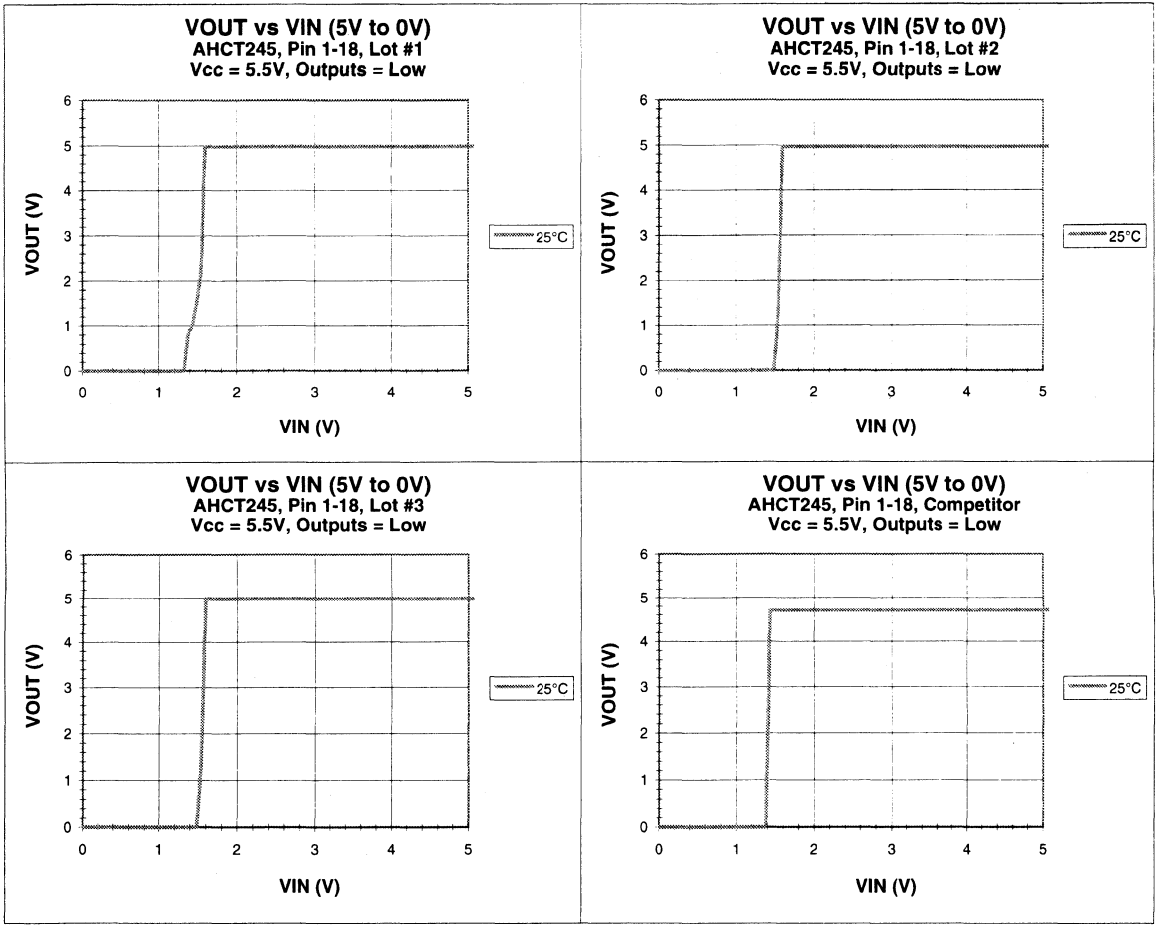

VOL vs IOL
AHCT245, Pin 18, Lot #1
Vcc = 5.5V
VOL (V)
3.00
2.50
2.00
1.50
1.00
0.50
0.00
0
10
20
30
40
50
60
70
IOL (mA)
25°C
VOL vs IOL
AHCT245, Pin 18, Lot #2
Vcc = 5.5V
VOL (V)
IOL (mA)
25°C
VOL vs IOL
AHCT245, Pin 18, Lot #3
Vcc = 5.5V
VOL (V)
IOL (mA)
25°C
VOL vs IOL
AHCT245, Pin 18, Competitor
Vcc = 5.5V
VOL (V)
IOL (mA)
25°C

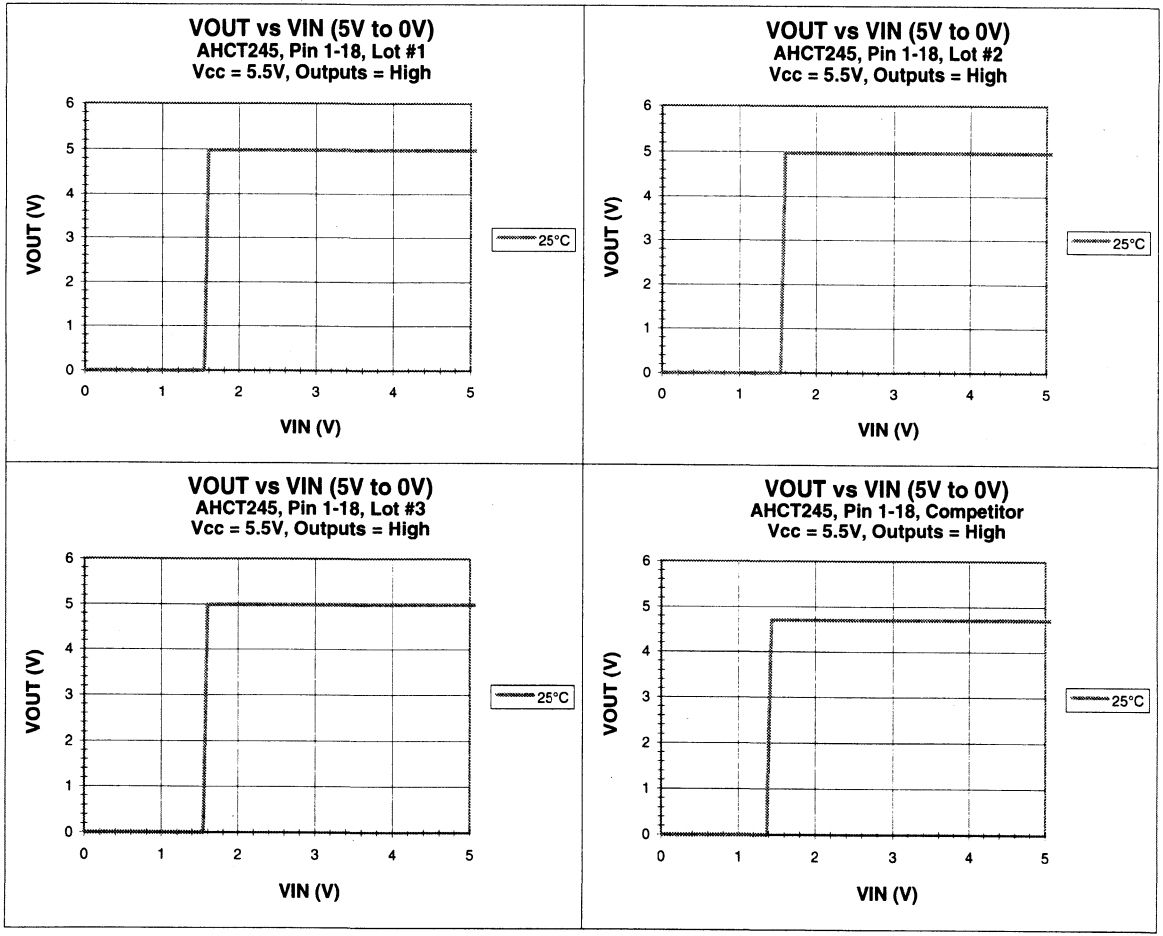

VOH vs IOH
AHCT245, Pin 18, Lot #1
Vcc = 4.5V
VOH (V)
IOH (mA)
25°C
VOH vs IOH
AHCT245, Pin 18, Lot #2
Vcc = 4.5V
VOH (V)
IOH (mA)
25°C
VOH vs IOH
AHCT245, Pin 18, Lot #3
Vcc = 4.5V
VOH (V)
IOH (mA)
25°C
VOH vs IOH
AHCT245, Pin 18, Competitor
Vcc = 4.5V
VOH (V)
IOH (mA)
25°C

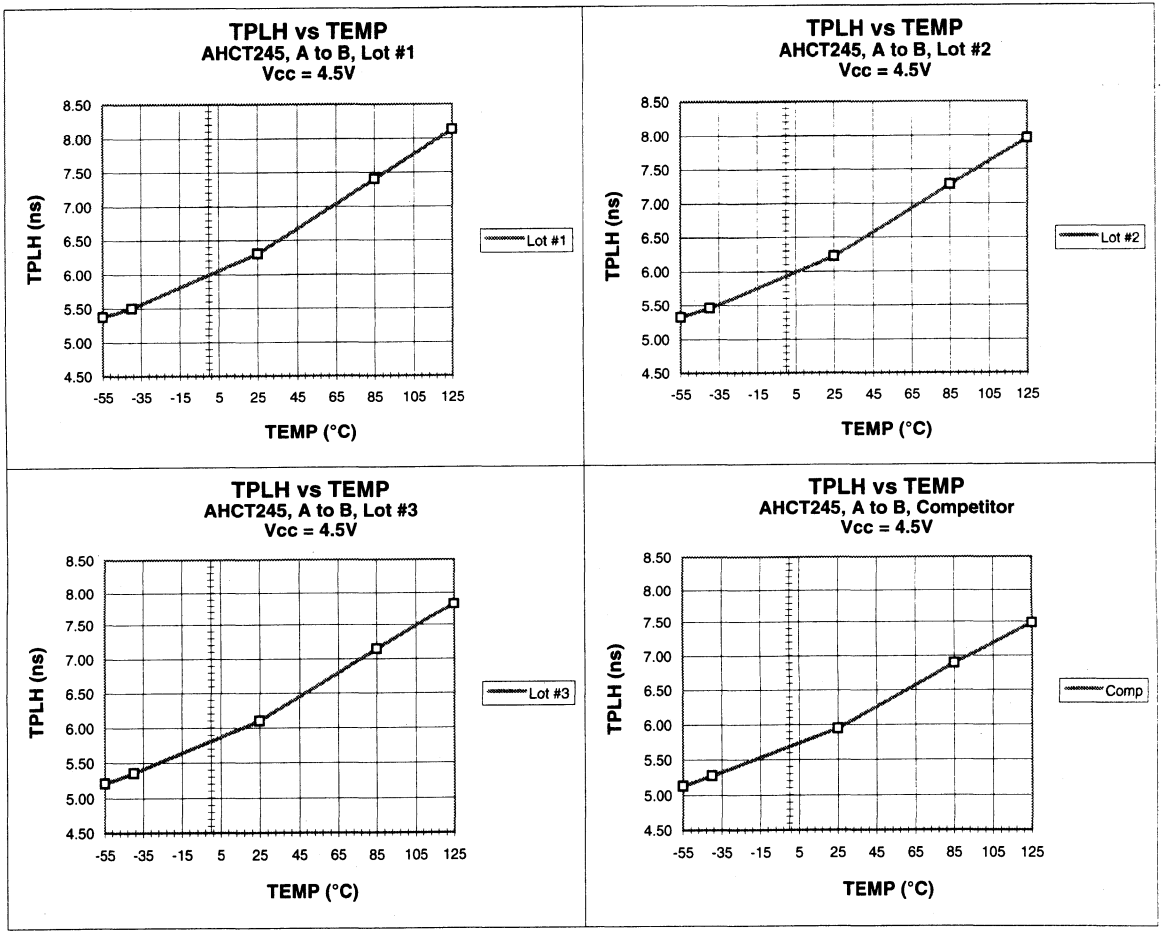

VOH vs IOH
AHCT245, Pin 18, Lot #1
Vcc = 5.5V
VOH (V)
IOH (mA)
25°C
VOH vs IOH
AHCT245, Pin 18, Lot #2
Vcc = 5.5V
VOH (V)
IOH (mA)
25°C
VOH vs IOH
AHCT245, Pin 18, Lot #3
Vcc = 5.5V
VOH (V)
IOH (mA)
25°C
VOH vs IOH
AHCT245, Pin 18, Competitor
Vcc = 5.5V
VOH (V)
IOH (mA)
25°C

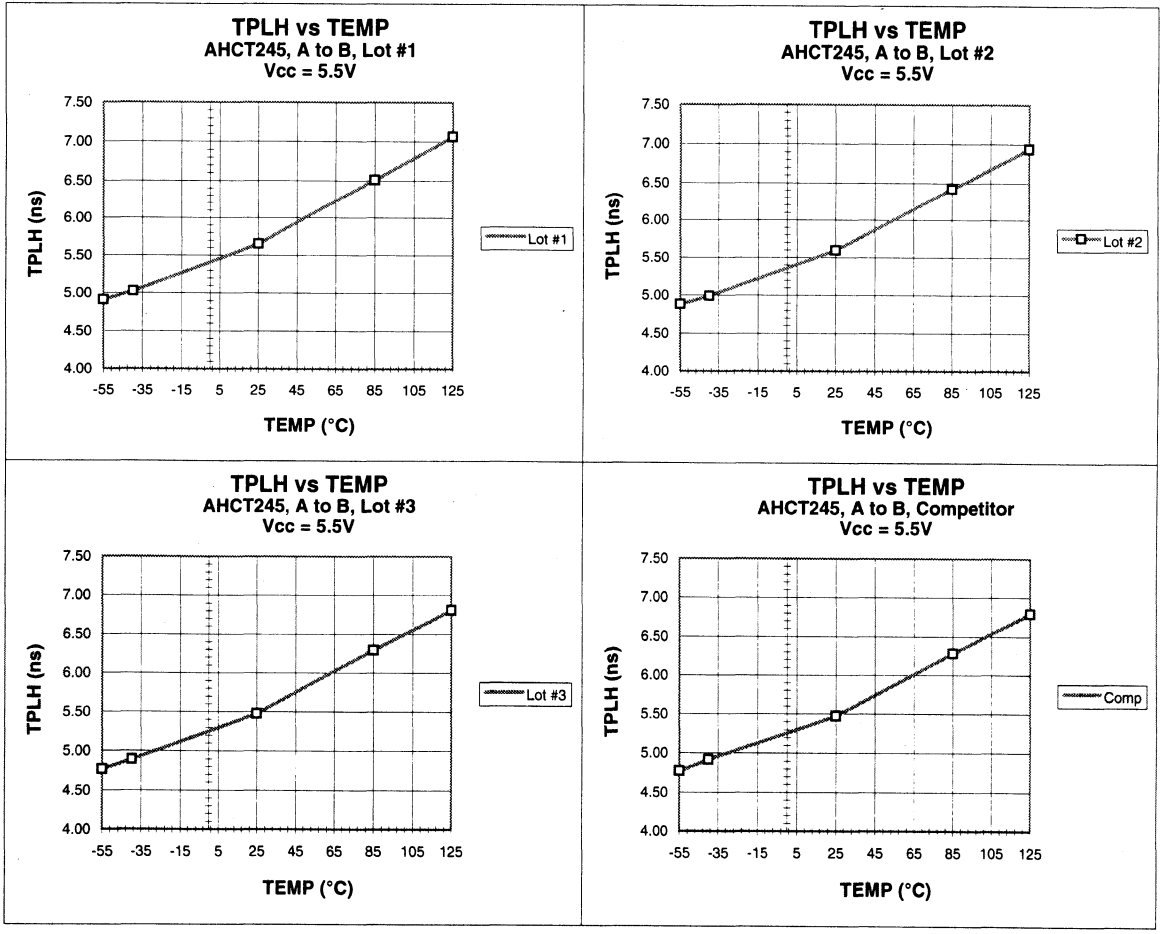

VOUT vs VIN (0V to 5V)
AHCT245, Pin 1-18, Lot #1
Vcc = 5.5V, Outputs = Low
VOUT (V)
VIN (V)
25°C
VOUT vs VIN (0V to 5V)
AHCT245, Pin 1-18, Lot #2
Vcc = 5.5V, Outputs = Low
VOUT (V)
VIN (V)
25°C
VOUT vs VIN (0V to 5V)
AHCT245, Pin 1-18, Lot #3
Vcc = 5.5V, Outputs = Low
VOUT (V)
VIN (V)
25°C
VOUT vs VIN (0V to 5V)
AHCT245, Pin 1-18, Competitor
Vcc = 5.5V, Outputs = Low
VOUT (V)
VIN (V)
25°C

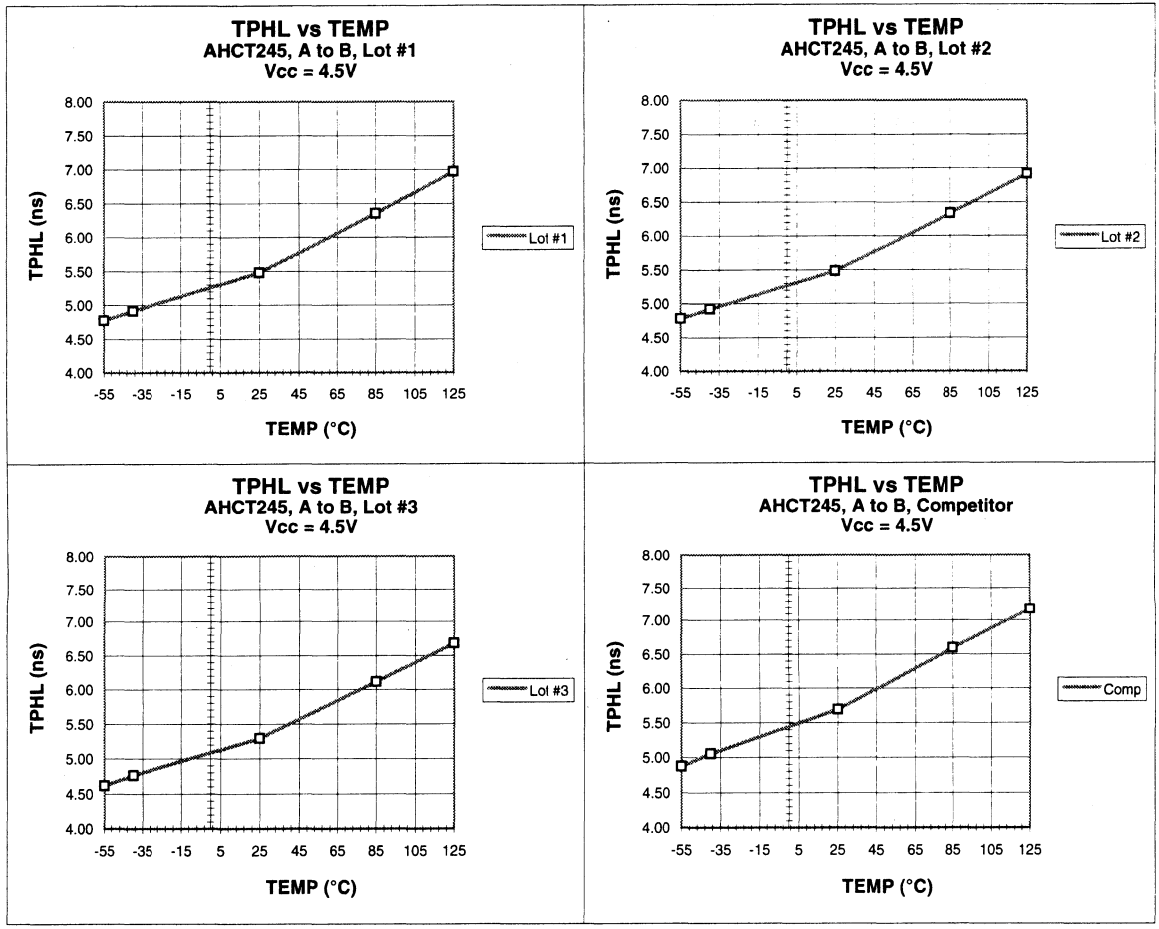

VOUT vs VIN (0V to 5V)
AHCT245, Pin 1-18, Lot #1
Vcc = 5.5V, Outputs = High
VOUT (V)
VIN (V)
25°C
VOUT vs VIN (0V to 5V)
AHCT245, Pin 1-18, Lot #2
Vcc = 5.5V, Outputs = High
VOUT (V)
VIN (V)
25°C
VOUT vs VIN (0V to 5V)
AHCT245, Pin 1-18, Lot #3
Vcc = 5.5V, Outputs = High
VOUT (V)
VIN (V)
25°C
VOUT vs VIN (0V to 5V)
AHCT245, Pin 1-18, Competitor
Vcc = 5.5V, Outputs = High
VOUT (V)
VIN (V)
25°C


VOUT vs VIN (5V to 0V)
AHCT245, Pin 1-18, Lot #1
Vcc = 5.5V, Outputs = Low
VOUT (V)
VIN (V)
25°C
VOUT vs VIN (5V to 0V)
AHCT245, Pin 1-18, Lot #2
Vcc = 5.5V, Outputs = Low
VOUT (V)
VIN (V)
25°C
VOUT vs VIN (5V to 0V)
AHCT245, Pin 1-18, Lot #3
Vcc = 5.5V, Outputs = Low
VOUT (V)
VIN (V)
25°C
VOUT vs VIN (5V to 0V)
AHCT245, Pin 1-18, Competitor
Vcc = 5.5V, Outputs = Low
VOUT (V)
VIN (V)
25°C


VOUT vs VIN (5V to 0V)
AHCT245, Pin 1-18, Lot #1
Vcc = 5.5V, Outputs = High
VOUT (V)
VIN (V)
25°C
VOUT vs VIN (5V to 0V)
AHCT245, Pin 1-18, Lot #2
Vcc = 5.5V, Outputs = High
VOUT (V)
VIN (V)
25°C
VOUT vs VIN (5V to 0V)
AHCT245, Pin 1-18, Lot #3
Vcc = 5.5V, Outputs = High
VOUT (V)
VIN (V)
25°C
VOUT vs VIN (5V to 0V)
AHCT245, Pin 1-18, Competitor
Vcc = 5.5V, Outputs = High
VOUT (V)
VIN (V)
25°C


TPLH vs TEMP
AHCT245, A to B, Lot #1
Vcc = 4.5V
TPLH (ns)
8.50
8.00
7.50
7.00
6.50
6.00
5.50
5.00
4.50
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Lot #1
TPLH vs TEMP
AHCT245, A to B, Lot #2
Vcc = 4.5V
TPLH (ns)
8.50
8.00
7.50
7.00
6.50
6.00
5.50
5.00
4.50
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Lot #2
TPLH vs TEMP
AHCT245, A to B, Lot #3
Vcc = 4.5V
TPLH (ns)
8.50
8.00
7.50
7.00
6.50
6.00
5.50
5.00
4.50
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Lot #3
TPLH vs TEMP
AHCT245, A to B, Competitor
Vcc = 4.5V
TPLH (ns)
8.50
8.00
7.50
7.00
6.50
6.00
5.50
5.00
4.50
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Comp


TPLH vs TEMP
AHCT245, A to B, Lot #1
Vcc = 5.5V
TPLH (ns)
7.50
7.00
6.50
6.00
5.50
5.00
4.50
4.00
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Lot #1
TPLH vs TEMP
AHCT245, A to B, Lot #2
Vcc = 5.5V
TPLH (ns)
7.50
7.00
6.50
6.00
5.50
5.00
4.50
4.00
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Lot #2
TPLH vs TEMP
AHCT245, A to B, Lot #3
Vcc = 5.5V
TPLH (ns)
7.50
7.00
6.50
6.00
5.50
5.00
4.50
4.00
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Lot #3
TPLH vs TEMP
AHCT245, A to B, Competitor
Vcc = 5.5V
TPLH (ns)
7.50
7.00
6.50
6.00
5.50
5.00
4.50
4.00
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Comp


TPHL vs TEMP
AHCT245, A to B, Lot #1
Vcc = 4.5V
TPHL (ns)
8.00
7.50
7.00
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-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Lot #1
TPHL vs TEMP
AHCT245, A to B, Lot #2
Vcc = 4.5V
TPHL (ns)
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-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Lot #2
TPHL vs TEMP
AHCT245, A to B, Lot #3
Vcc = 4.5V
TPHL (ns)
8.00
7.50
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-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Lot #3
TPHL vs TEMP
AHCT245, A to B, Competitor
Vcc = 4.5V
TPHL (ns)
8.00
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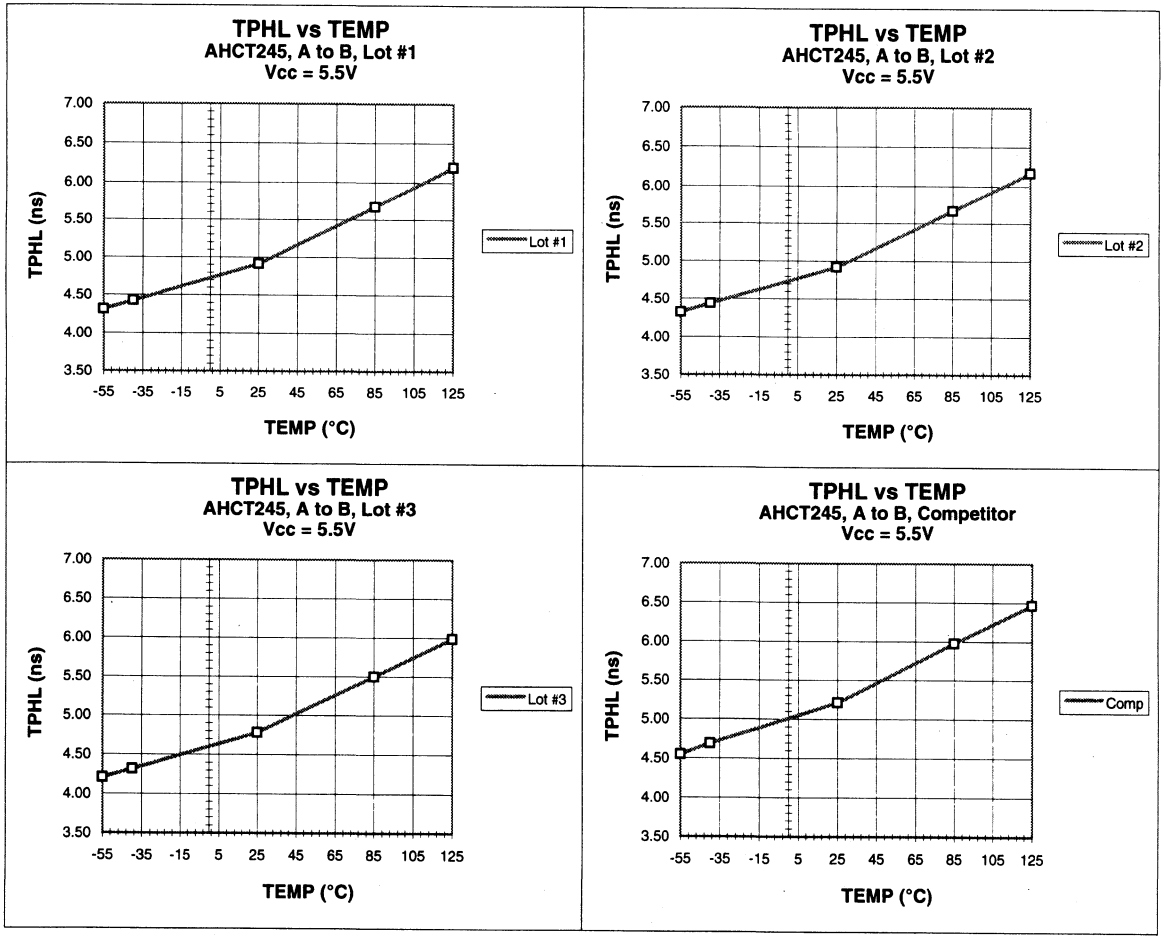
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Comp


TPHL vs TEMP
AHCT245, A to B, Lot #1
Vcc = 5.5V
TPHL (ns)
7.00
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-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Lot #1
TPHL vs TEMP
AHCT245, A to B, Lot #2
Vcc = 5.5V
TPHL (ns)
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-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Lot #2
TPHL vs TEMP
AHCT245, A to B, Lot #3
Vcc = 5.5V
TPHL (ns)
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-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Lot #3
TPHL vs TEMP
AHCT245, A to B, Competitor
Vcc = 5.5V
TPHL (ns)
7.00
6.50
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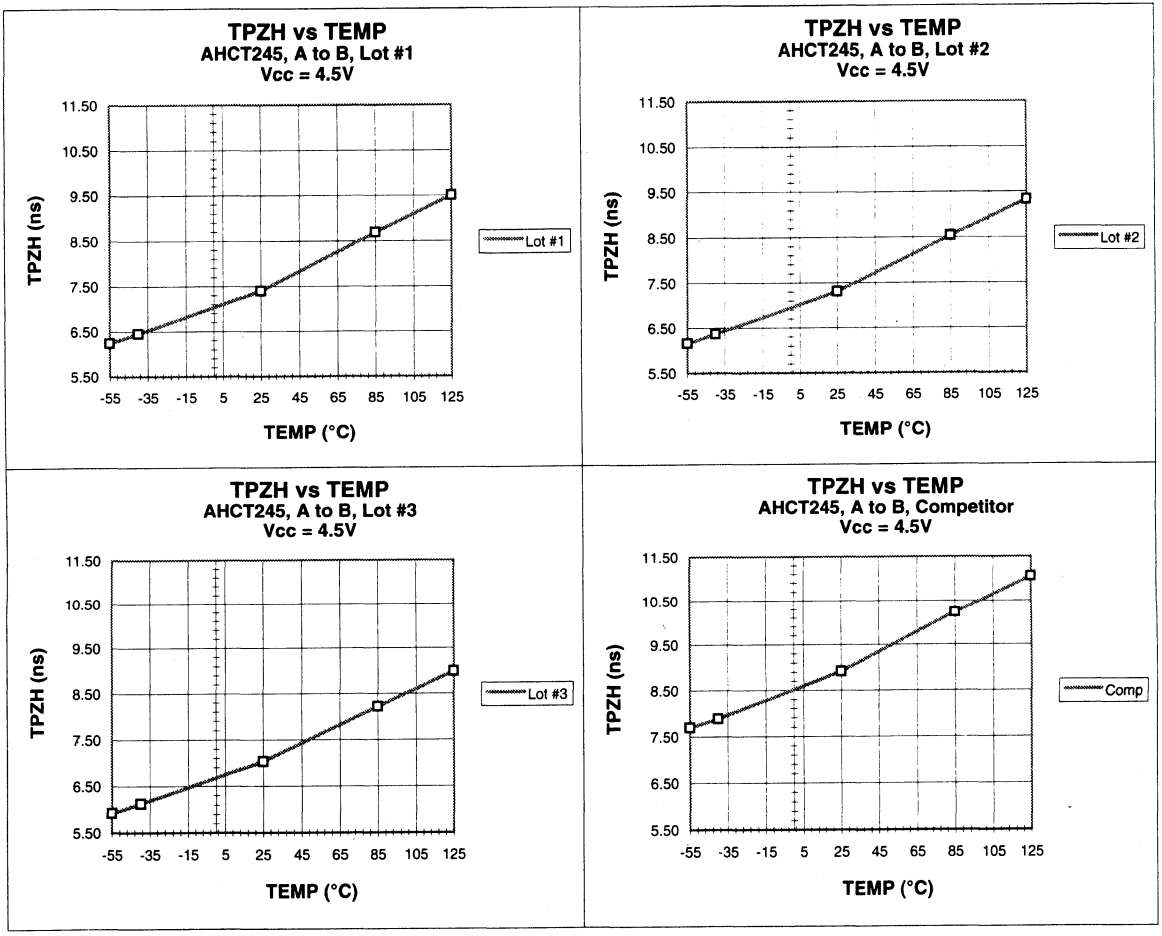
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Comp


TPZH vs TEMP
AHCT245, A to B, Lot #1
Vcc = 4.5V
TPZH (ns)
11.50
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8.50
7.50
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-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Lot #1
TPZH vs TEMP
AHCT245, A to B, Lot #2
Vcc = 4.5V
TPZH (ns)
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7.50
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-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Lot #2
TPZH vs TEMP
AHCT245, A to B, Lot #3
Vcc = 4.5V
TPZH (ns)
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-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Lot #3
TPZH vs TEMP
AHCT245, A to B, Competitor
Vcc = 4.5V
TPZH (ns)
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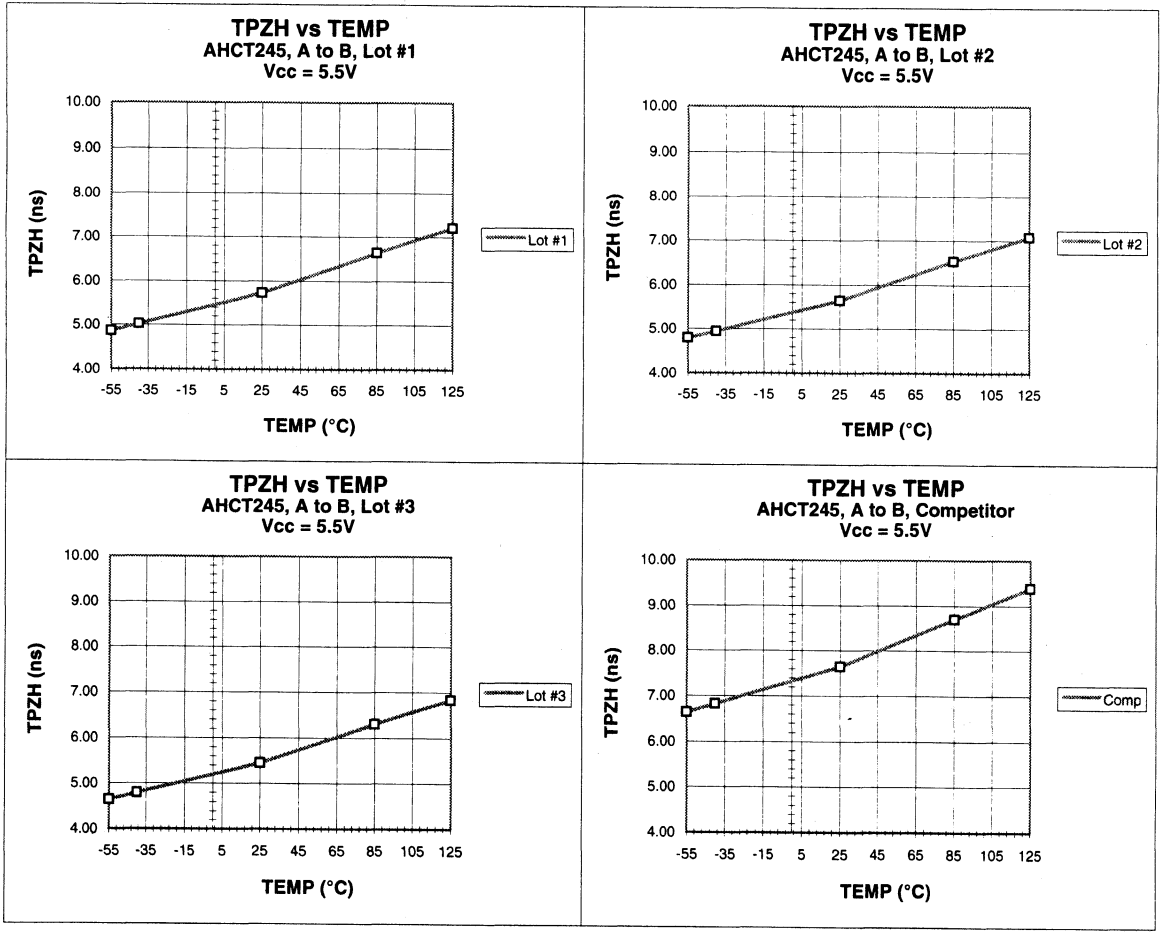
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Comp


TPZH vs TEMP
AHCT245, A to B, Lot #1
Vcc = 5.5V
TPZH (ns)
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-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Lot #1
TPZH vs TEMP
AHCT245, A to B, Lot #2
Vcc = 5.5V
TPZH (ns)
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-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Lot #2
TPZH vs TEMP
AHCT245, A to B, Lot #3
Vcc = 5.5V
TPZH (ns)
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-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Lot #3
TPZH vs TEMP
AHCT245, A to B, Competitor
Vcc = 5.5V
TPZH (ns)
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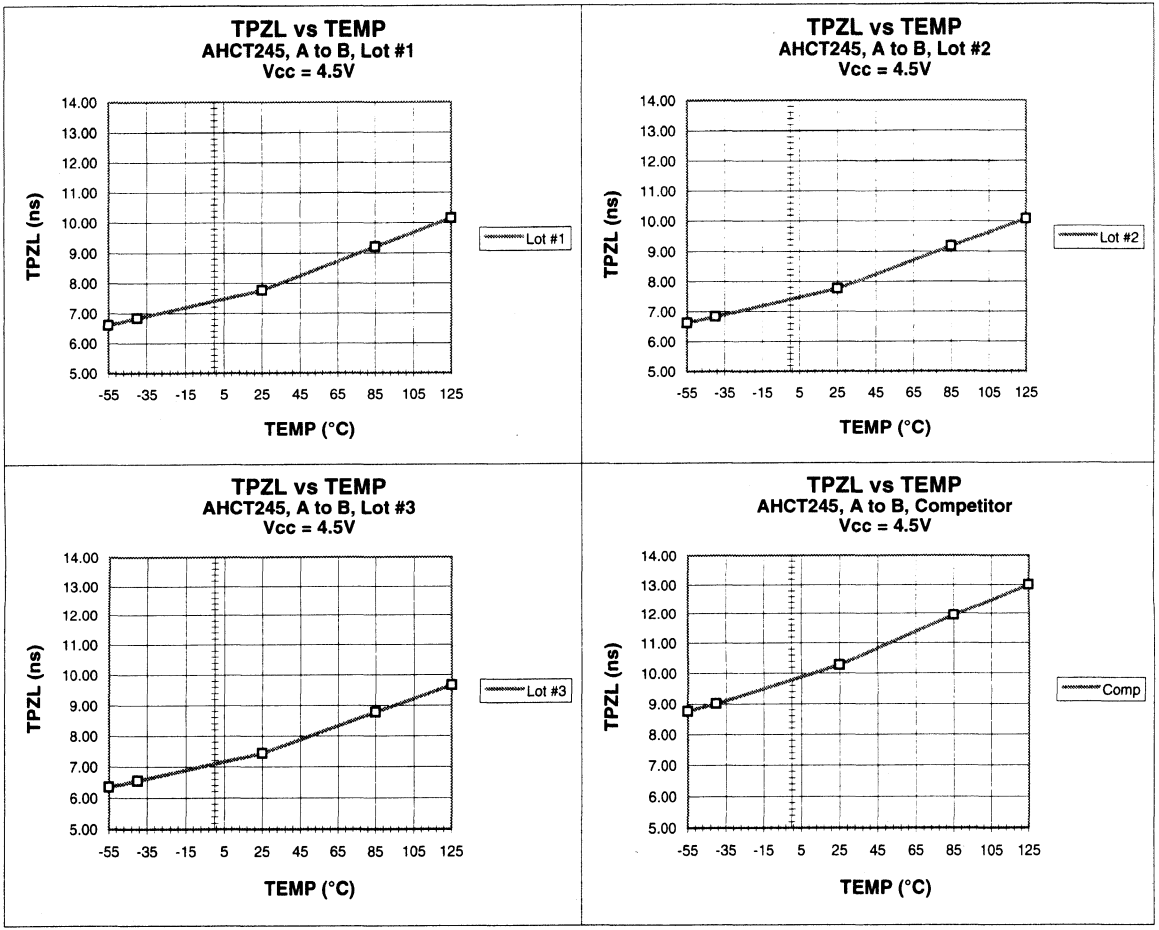
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Comp


TPZL vs TEMP
AHCT245, A to B, Lot #1
Vcc = 4.5V
TPZL (ns)
14.00
13.00
12.00
11.00
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5.00
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Lot #1
TPZL vs TEMP
AHCT245, A to B, Lot #2
Vcc = 4.5V
TPZL (ns)
14.00
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-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Lot #2
TPZL vs TEMP
AHCT245, A to B, Lot #3
Vcc = 4.5V
TPZL (ns)
14.00
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-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Lot #3
TPZL vs TEMP
AHCT245, A to B, Competitor
Vcc = 4.5V
TPZL (ns)
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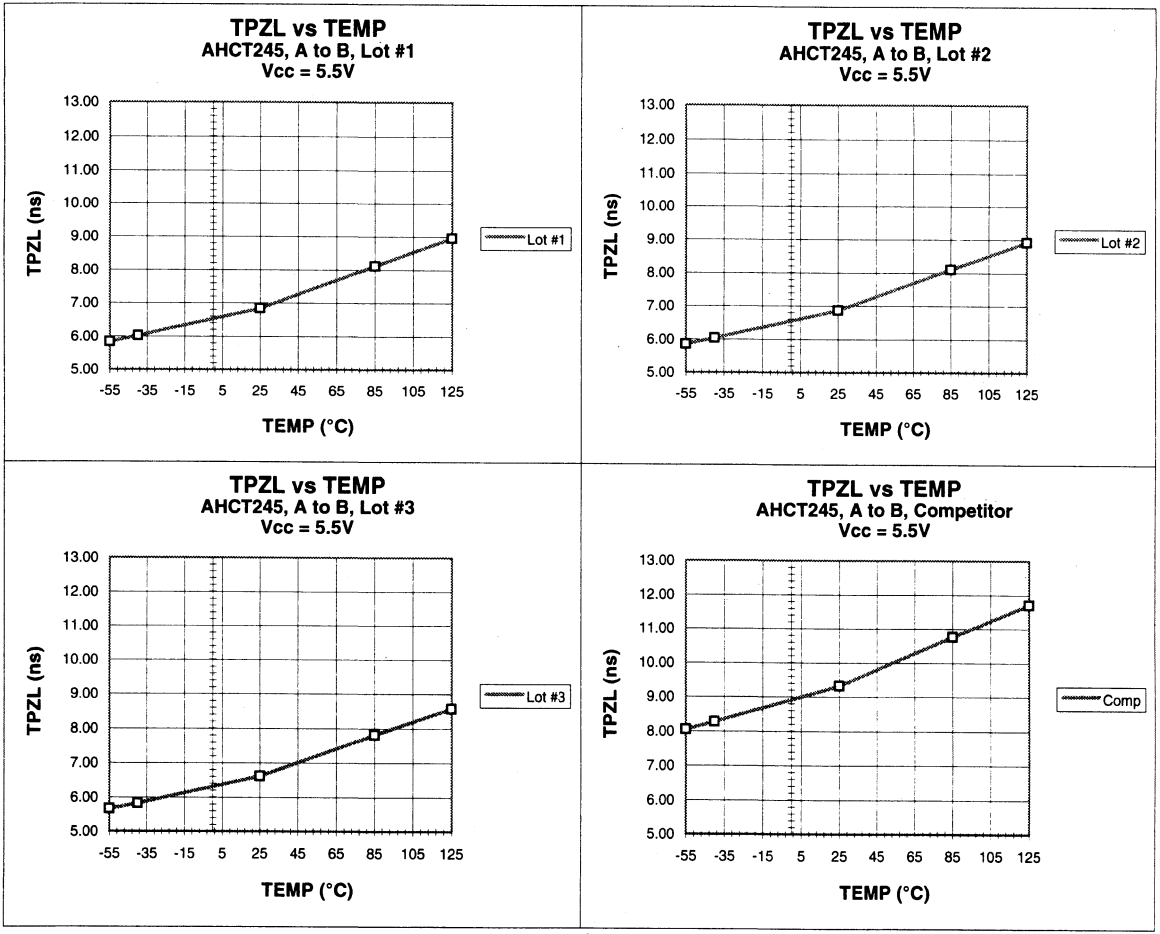
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Comp


TPZL vs TEMP
AHCT245, A to B, Lot #1
Vcc = 5.5V
TPZL (ns)
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-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Lot #1
TPZL vs TEMP
AHCT245, A to B, Lot #2
Vcc = 5.5V
TPZL (ns)
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-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Lot #2
TPZL vs TEMP
AHCT245, A to B, Lot #3
Vcc = 5.5V
TPZL (ns)
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-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Lot #3
TPZL vs TEMP
AHCT245, A to B, Competitor
Vcc = 5.5V
TPZL (ns)
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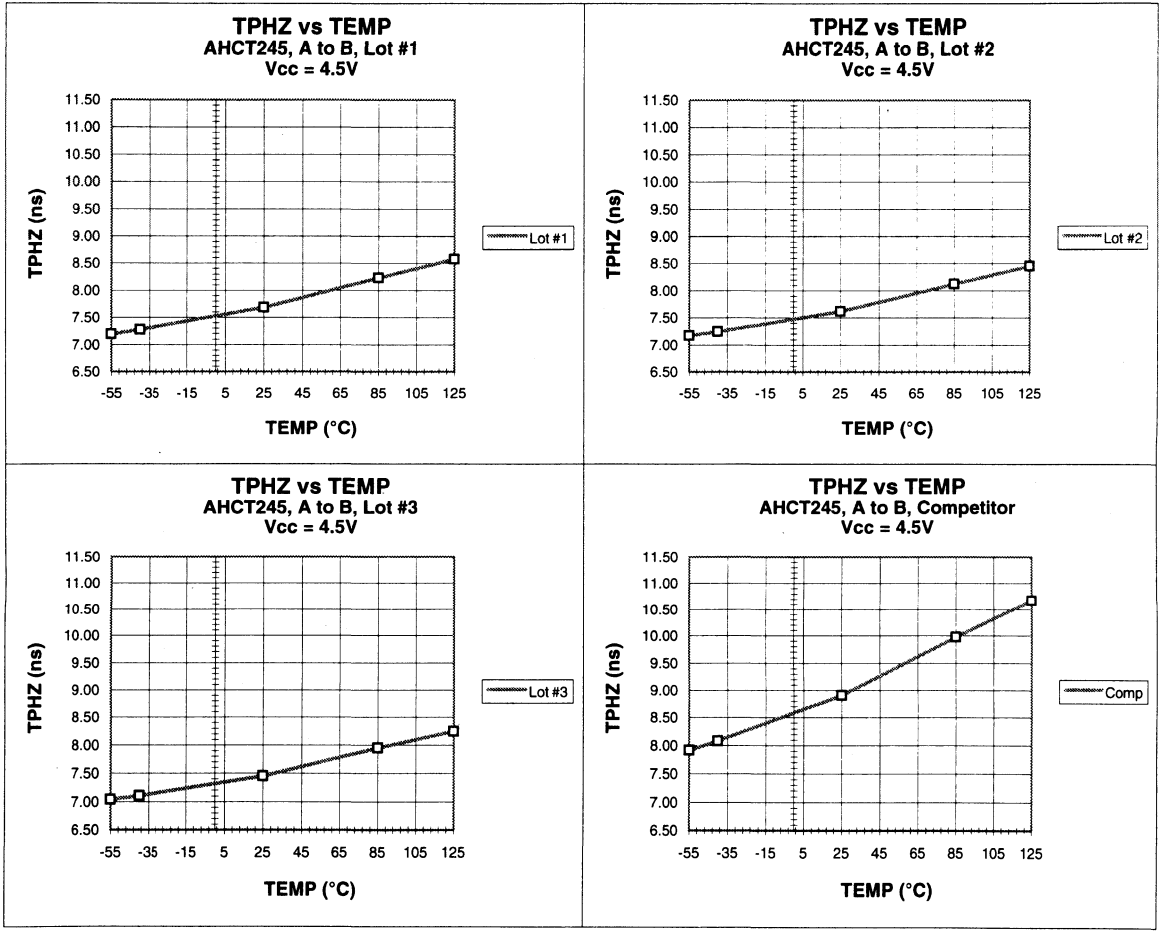
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Comp


TPHZ vs TEMP
AHCT245, A to B, Lot #1
Vcc = 4.5V
TPHZ (ns)
11.50
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-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Lot #1
TPHZ vs TEMP
AHCT245, A to B, Lot #2
Vcc = 4.5V
TPHZ (ns)
11.50
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6.50
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Lot #2
TPHZ vs TEMP
AHCT245, A to B, Lot #3
Vcc = 4.5V
TPHZ (ns)
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-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Lot #3
TPHZ vs TEMP
AHCT245, A to B, Competitor
Vcc = 4.5V
TPHZ (ns)
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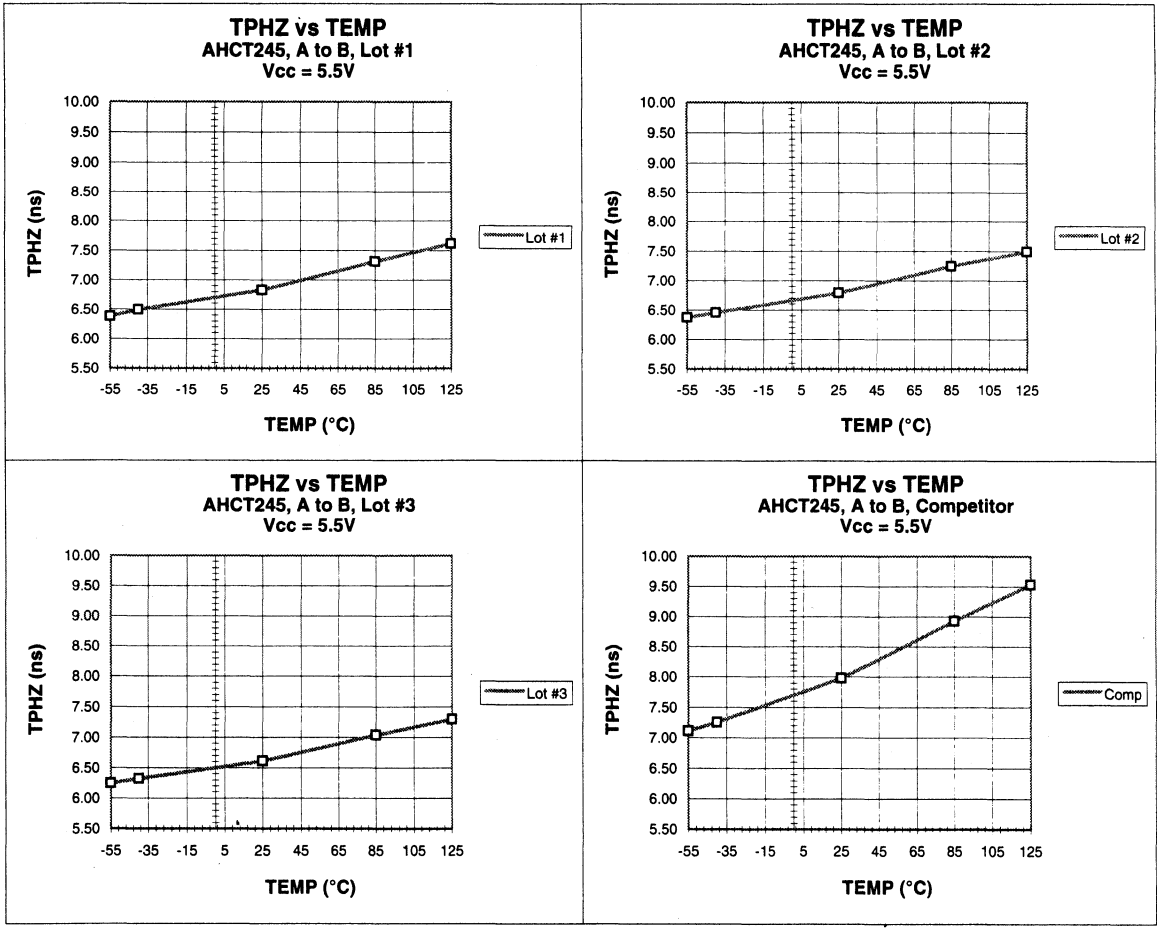
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Comp


TPHZ vs TEMP
AHCT245, A to B, Lot #1
Vcc = 5.5V
TPHZ (ns)
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-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Lot #1
TPHZ vs TEMP
AHCT245, A to B, Lot #2
Vcc = 5.5V
TPHZ (ns)
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-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Lot #2
TPHZ vs TEMP
AHCT245, A to B, Lot #3
Vcc = 5.5V
TPHZ (ns)
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-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Lot #3
TPHZ vs TEMP
AHCT245, A to B, Competitor
Vcc = 5.5V
TPHZ (ns)
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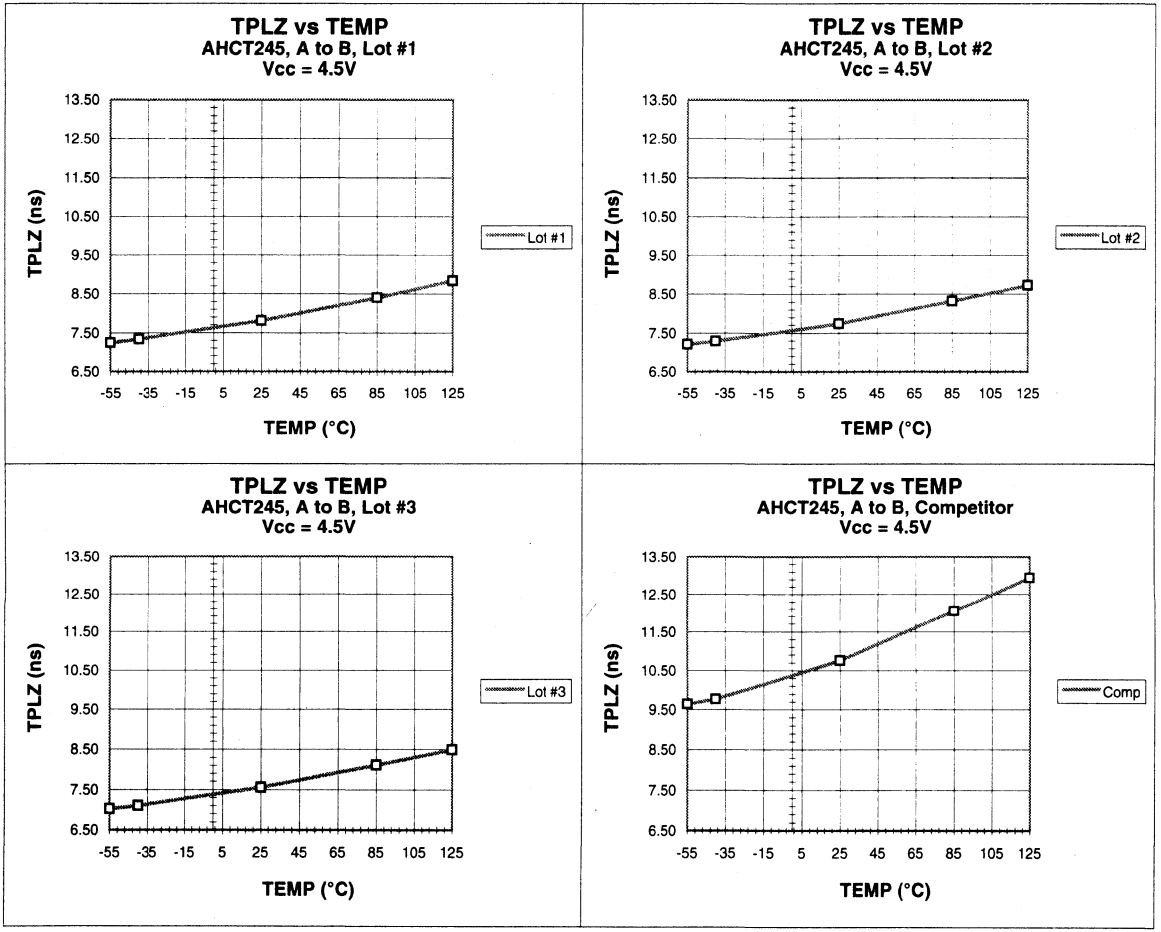
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Comp


TPLZ vs TEMP
AHCT245, A to B, Lot #1
Vcc = 4.5V
TPLZ (ns)
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-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Lot #1
TPLZ vs TEMP
AHCT245, A to B, Lot #2
Vcc = 4.5V
TPLZ (ns)
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-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Lot #2
TPLZ vs TEMP
AHCT245, A to B, Lot #3
Vcc = 4.5V
TPLZ (ns)
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-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Lot #3
TPLZ vs TEMP
AHCT245, A to B, Competitor
Vcc = 4.5V
TPLZ (ns)
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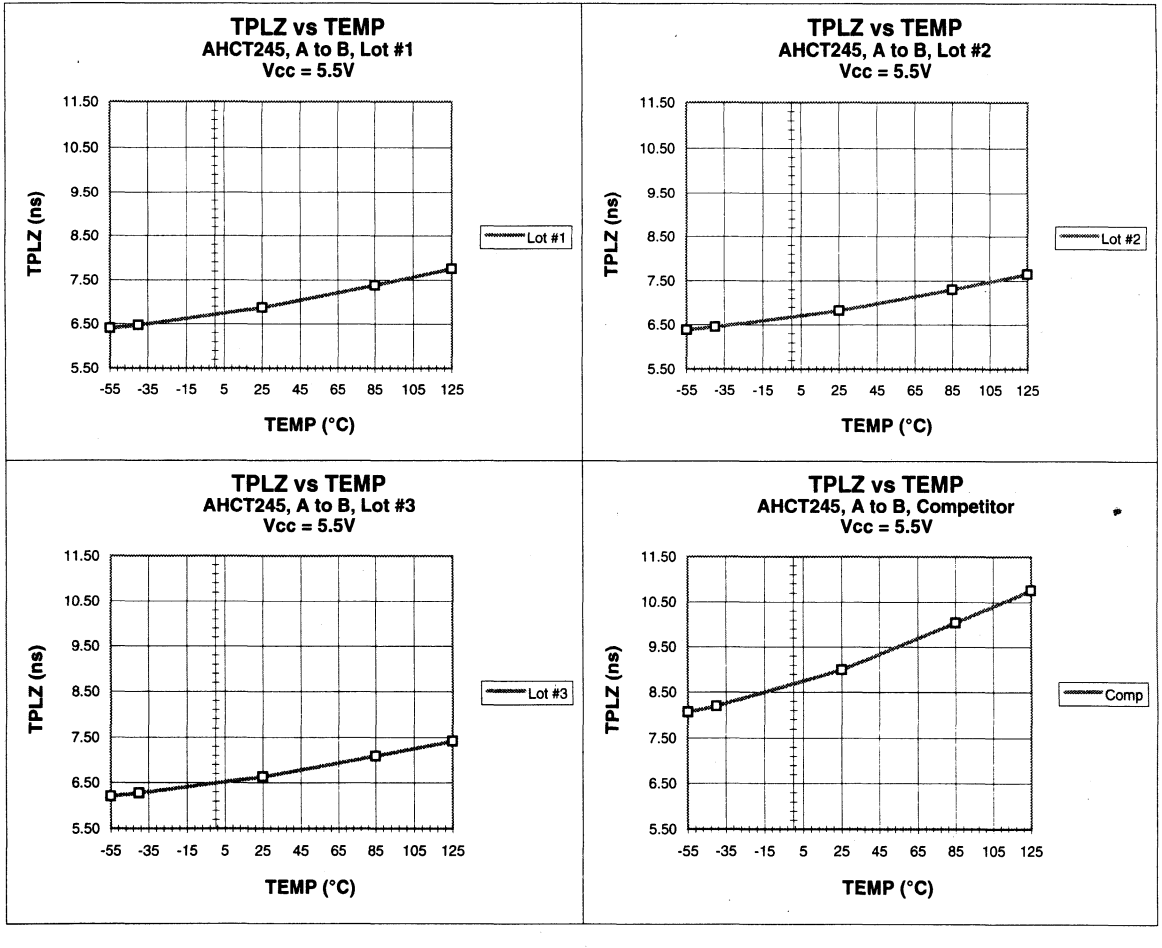
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Comp


TPLZ vs TEMP
AHCT245, A to B, Lot #1
Vcc = 5.5V
TPLZ (ns)
11.50
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-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Lot #1
TPLZ vs TEMP
AHCT245, A to B, Lot #2
Vcc = 5.5V
TPLZ (ns)
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-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Lot #2
TPLZ vs TEMP
AHCT245, A to B, Lot #3
Vcc = 5.5V
TPLZ (ns)
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-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Lot #3
TPLZ vs TEMP
AHCT245, A to B, Competitor
Vcc = 5.5V
TPLZ (ns)
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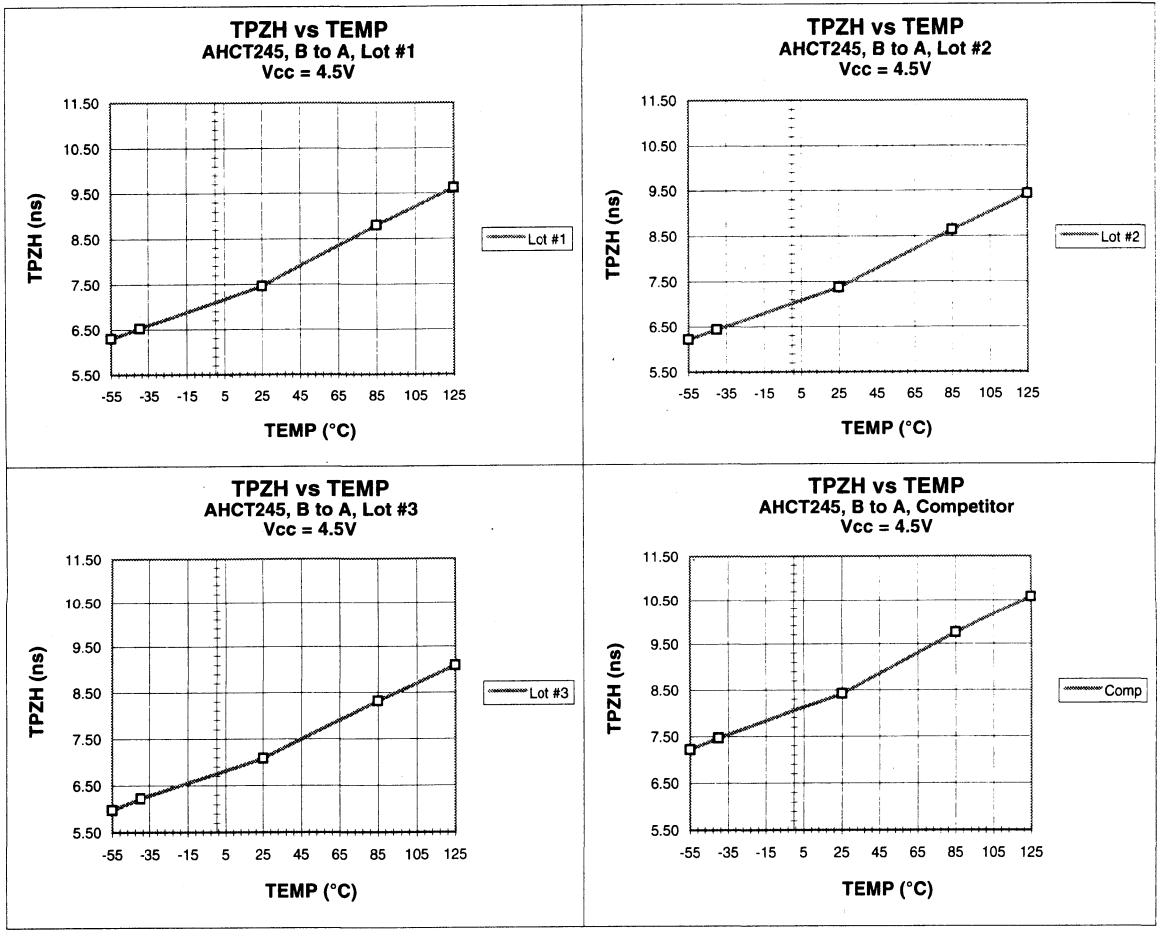
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Comp


TPZH vs TEMP
AHCT245, B to A, Lot #1
Vcc = 4.5V
TPZH (ns)
11.50
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-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Lot #1
TPZH vs TEMP
AHCT245, B to A, Lot #2
Vcc = 4.5V
TPZH (ns)
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-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Lot #2
TPZH vs TEMP
AHCT245, B to A, Lot #3
Vcc = 4.5V
TPZH (ns)
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-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Lot #3
TPZH vs TEMP
AHCT245, B to A, Competitor
Vcc = 4.5V
TPZH (ns)
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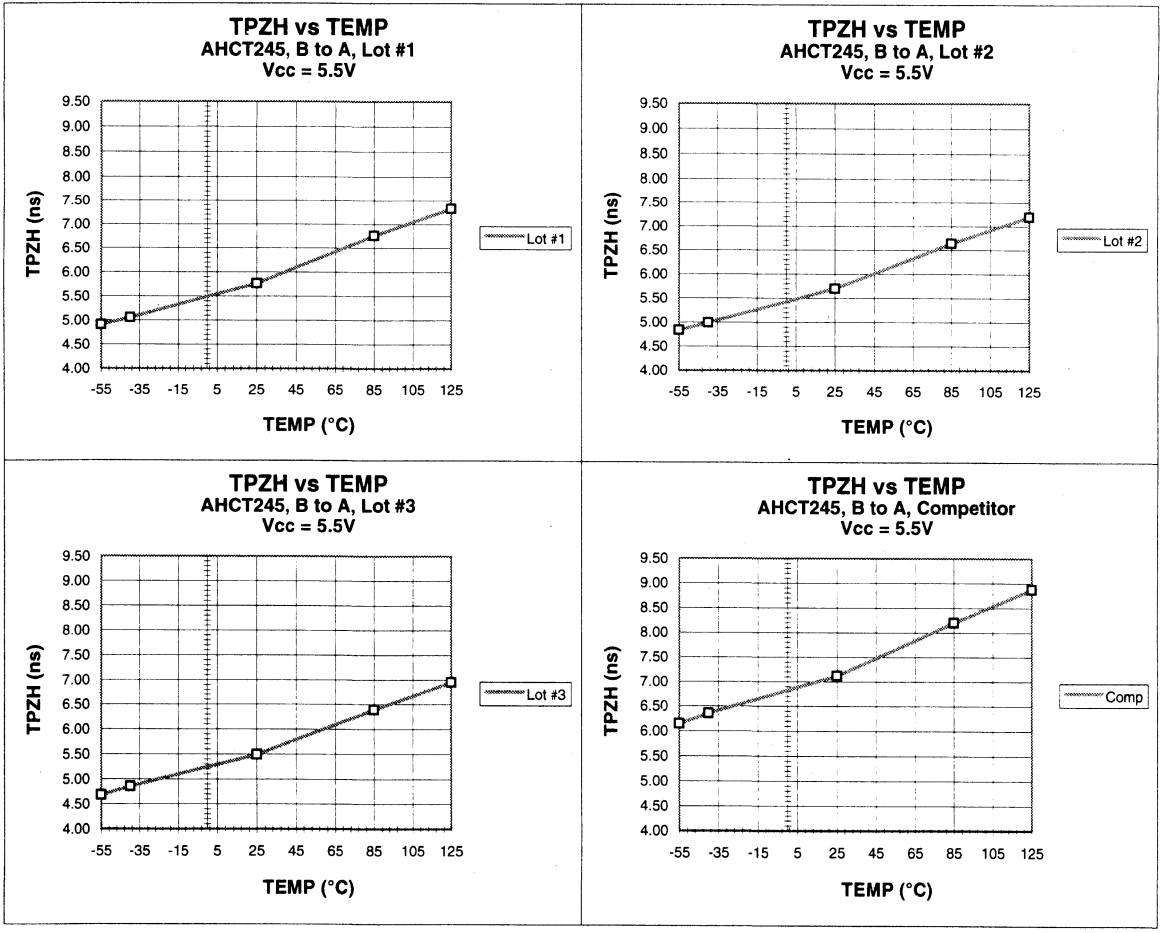
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Comp


TPZH vs TEMP
AHCT245, B to A, Lot #1
Vcc = 5.5V
TPZH (ns)
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-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Lot #1
TPZH vs TEMP
AHCT245, B to A, Lot #2
Vcc = 5.5V
TPZH (ns)
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-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Lot #2
TPZH vs TEMP
AHCT245, B to A, Lot #3
Vcc = 5.5V
TPZH (ns)
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-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Lot #3
TPZH vs TEMP
AHCT245, B to A, Competitor
Vcc = 5.5V
TPZH (ns)
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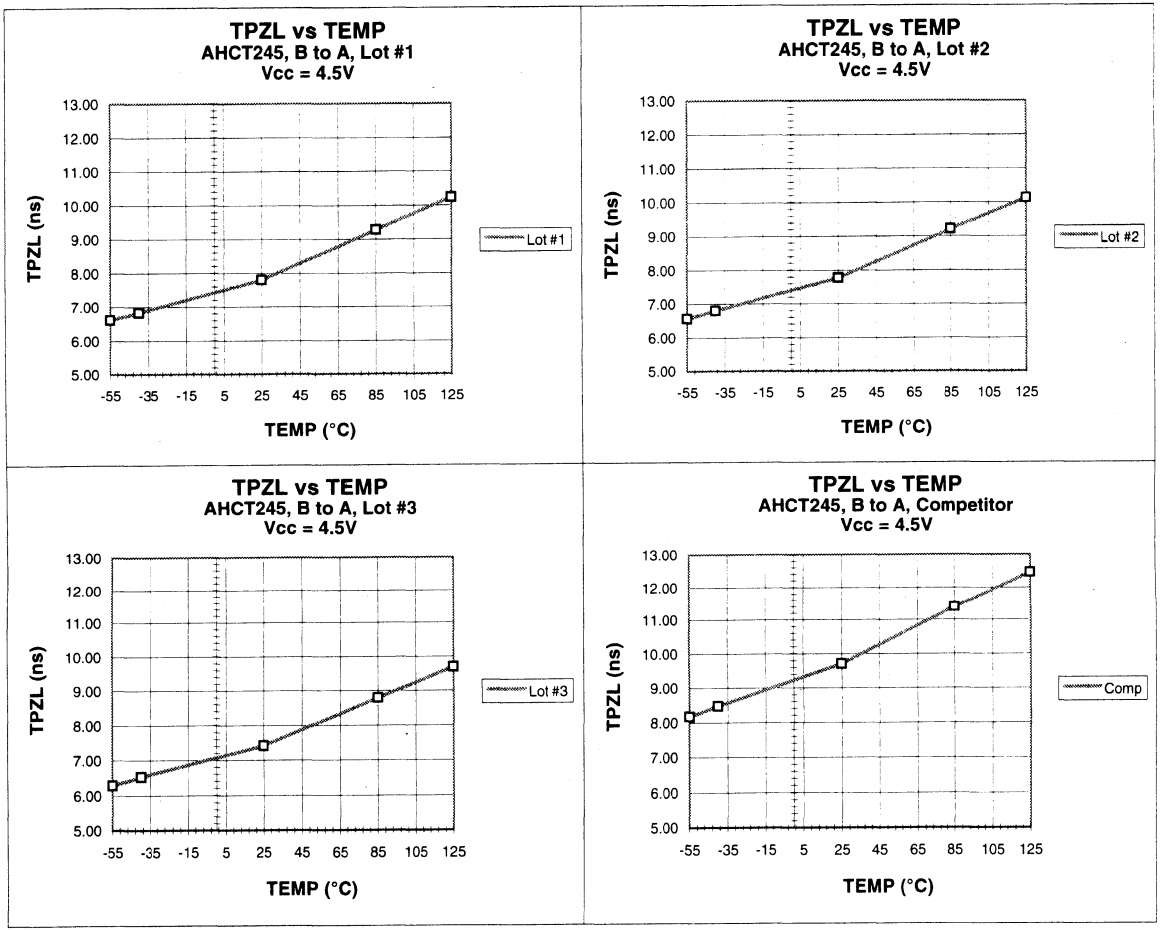
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Comp


TPZL vs TEMP
AHCT245, B to A, Lot #1
Vcc = 4.5V
TPZL (ns)
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12.00
11.00
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-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Lot #1
TPZL vs TEMP
AHCT245, B to A, Lot #2
Vcc = 4.5V
TPZL (ns)
13.00
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-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Lot #2
TPZL vs TEMP
AHCT245, B to A, Lot #3
Vcc = 4.5V
TPZL (ns)
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-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Lot #3
TPZL vs TEMP
AHCT245, B to A, Competitor
Vcc = 4.5V
TPZL (ns)
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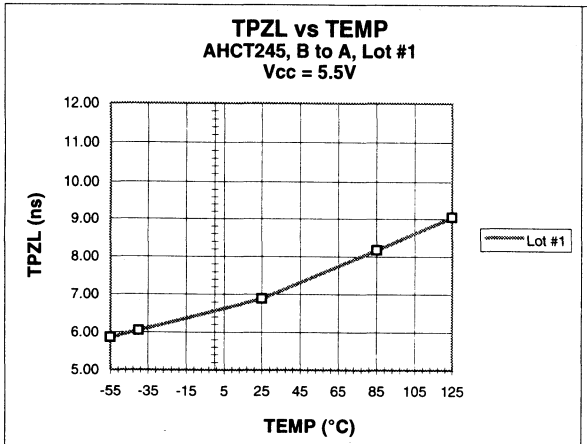
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Comp


TPZL vs TEMP
AHCT245, B to A, Lot #1
Vcc = 5.5V
TPZL (ns)
12.00
11.00
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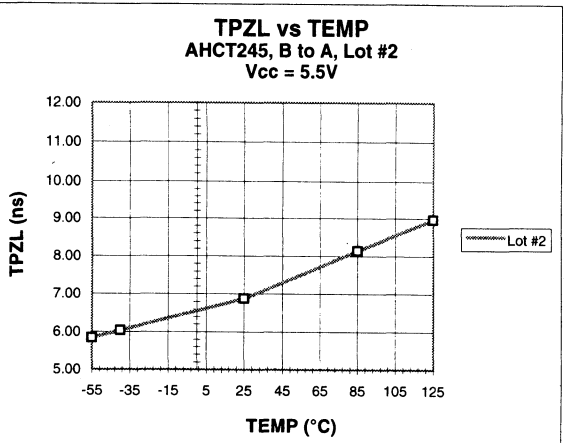
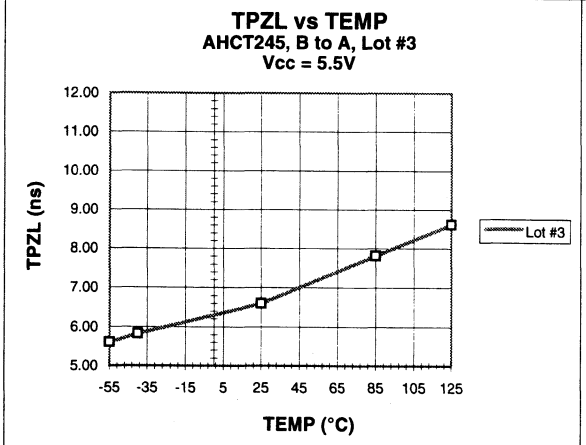
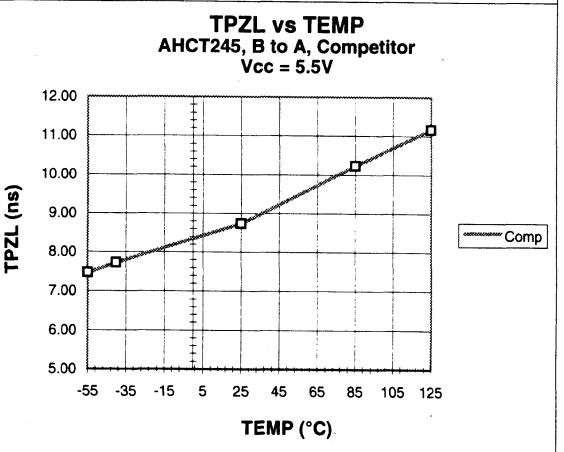
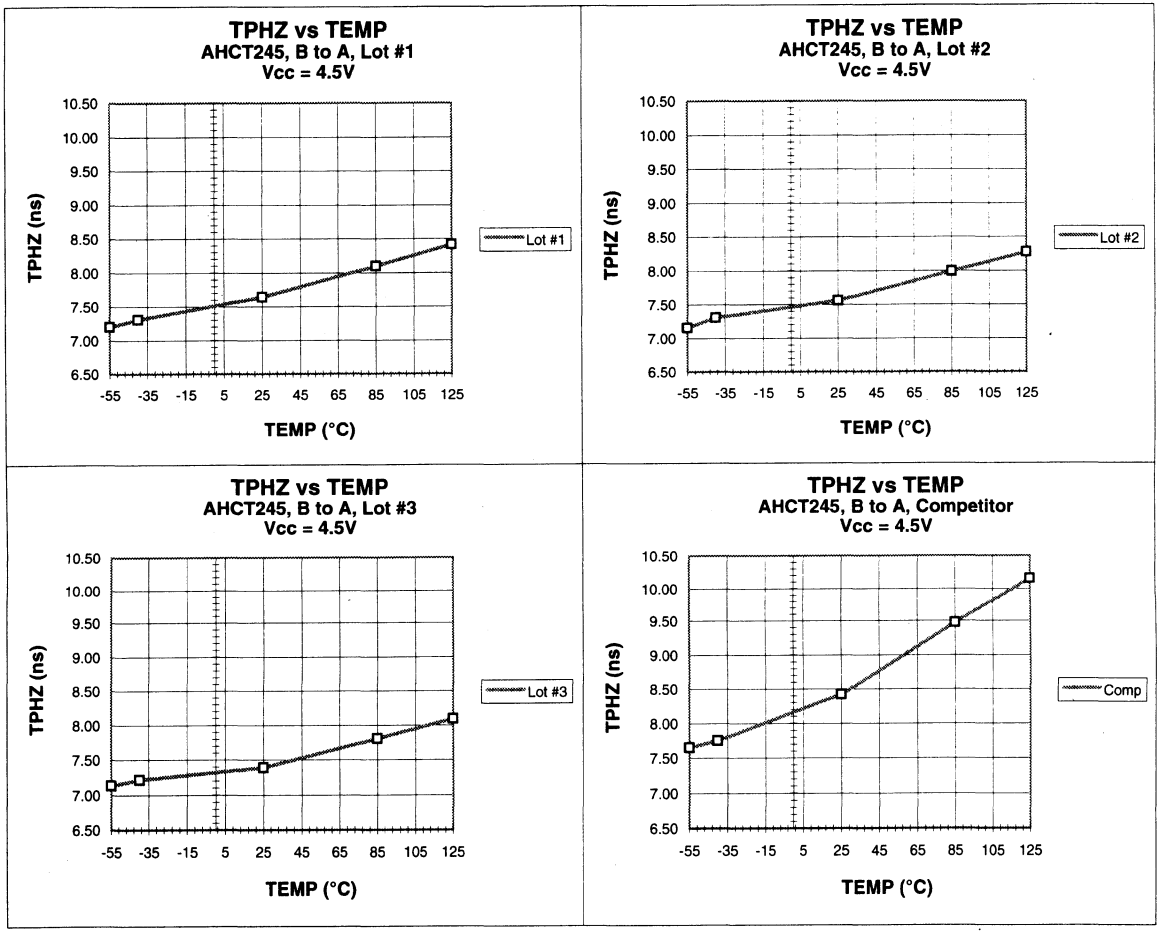
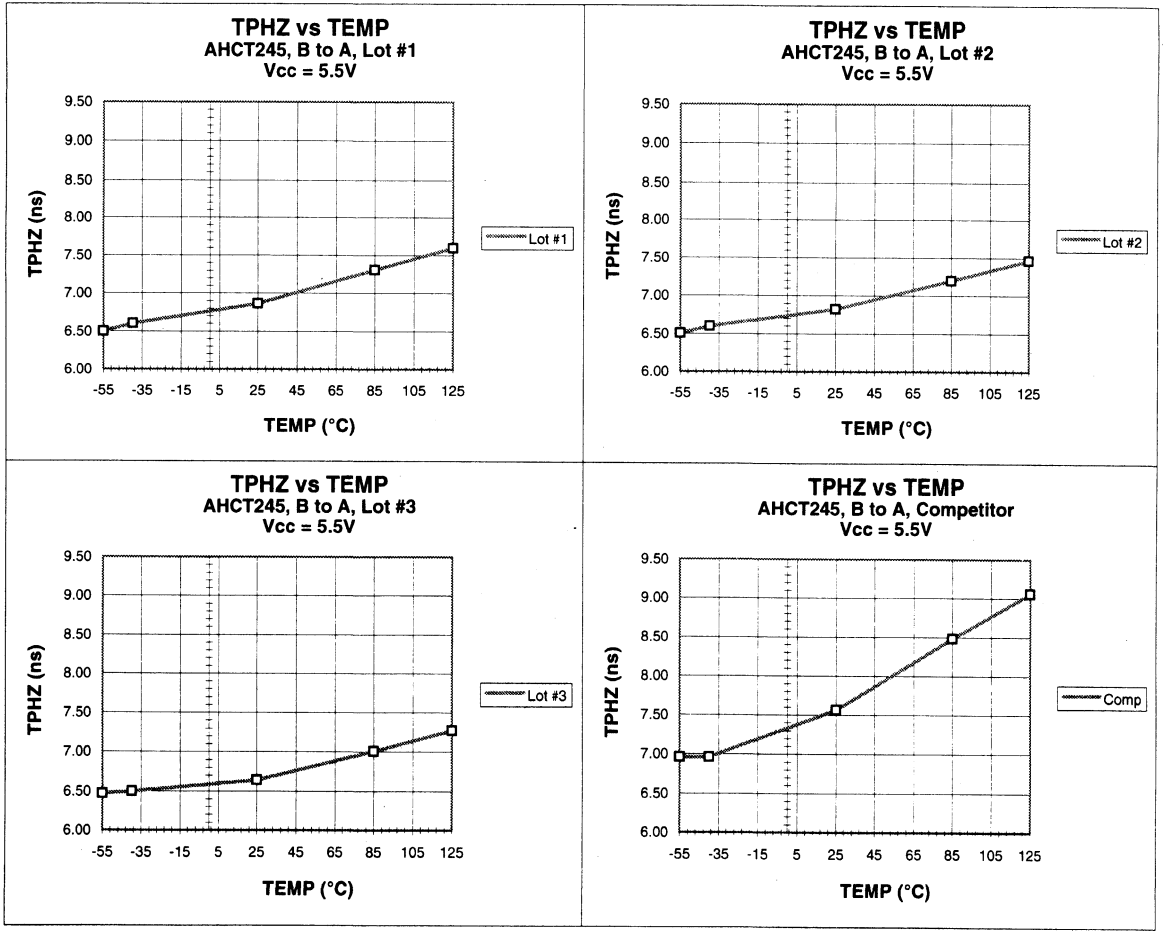
8.00
7.00
6.00
5.00
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Lot #1

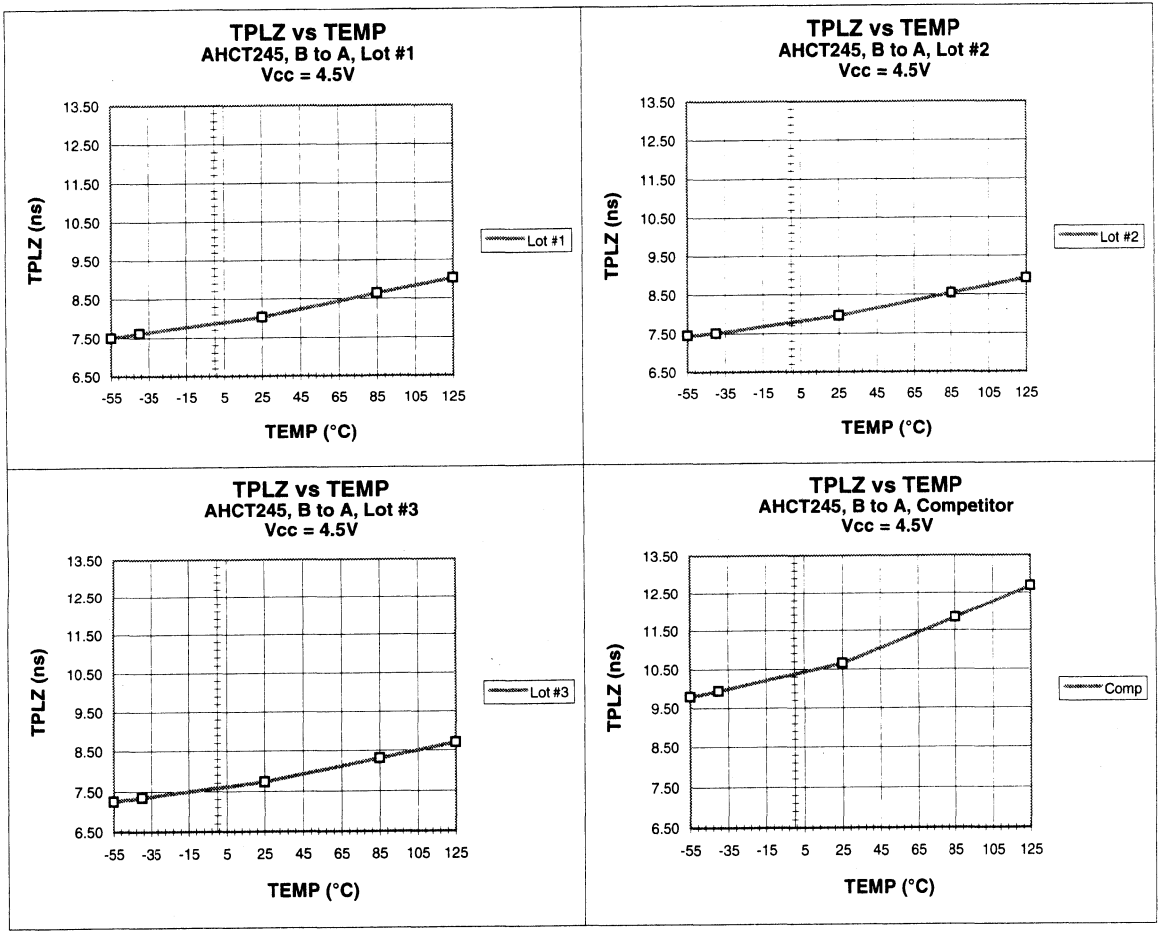

TPZL vs TEMP
AHCT245, B to A, Lot #2
Vcc = 5.5V
TPZL (ns)
12.00
11.00
10.00
9.00
8.00
7.00
6.00
5.00
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Lot #2

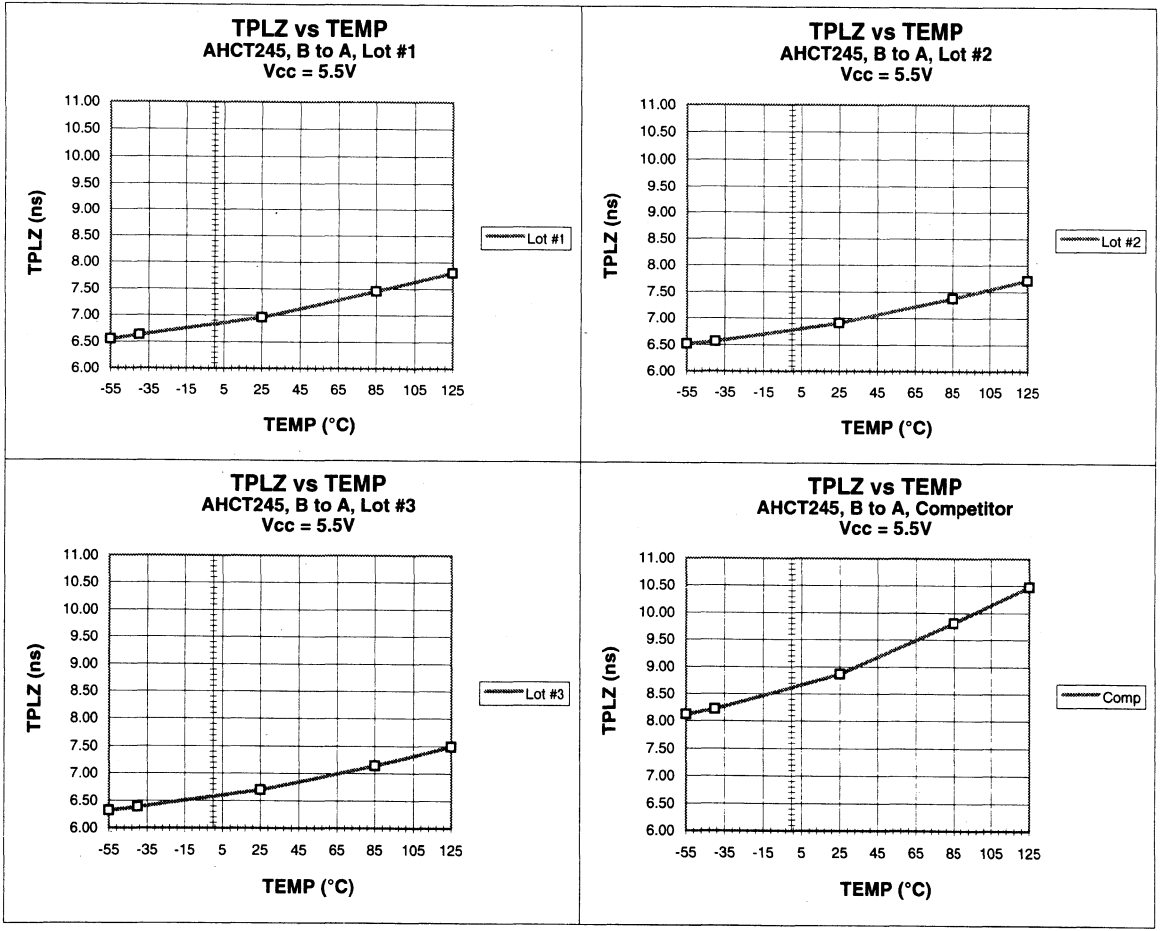

TPZL vs TEMP
AHCT245, B to A, Lot #3
Vcc = 5.5V
TPZL (ns)
12.00
11.00
10.00
9.00
8.00
7.00
6.00
5.00
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Lot #3


TPZL vs TEMP
AHCT245, B to A, Competitor
Vcc = 5.5V
TPZL (ns)
12.00
11.00
10.00
9.00
8.00
7.00
6.00
5.00
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Comp


TPHZ vs TEMP
AHCT245, B to A, Lot #1
Vcc = 4.5V
TPHZ (ns)
10.50
10.00
9.50
9.00
8.50
8.00
7.50
7.00
6.50
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Lot #1
TPHZ vs TEMP
AHCT245, B to A, Lot #2
Vcc = 4.5V
TPHZ (ns)
10.50
10.00
9.50
9.00
8.50
8.00
7.50
7.00
6.50
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Lot #2
TPHZ vs TEMP
AHCT245, B to A, Lot #3
Vcc = 4.5V
TPHZ (ns)
10.50
10.00
9.50
9.00
8.50
8.00
7.50
7.00
6.50
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Lot #3
TPHZ vs TEMP
AHCT245, B to A, Competitor
Vcc = 4.5V
TPHZ (ns)
10.50
10.00
9.50
9.00
8.50
8.00
7.50
7.00
6.50
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Comp


TPHZ vs TEMP
AHCT245, B to A, Lot #1
Vcc = 5.5V
TPHZ (ns)
9.50
9.00
8.50
8.00
7.50
7.00
6.50
6.00
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Lot #1
TPHZ vs TEMP
AHCT245, B to A, Lot #2
Vcc = 5.5V
TPHZ (ns)
9.50
9.00
8.50
8.00
7.50
7.00
6.50
6.00
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Lot #2
TPHZ vs TEMP
AHCT245, B to A, Lot #3
Vcc = 5.5V
TPHZ (ns)
9.50
9.00
8.50
8.00
7.50
7.00
6.50
6.00
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Lot #3
TPHZ vs TEMP
AHCT245, B to A, Competitor
Vcc = 5.5V
TPHZ (ns)
9.50
9.00
8.50
8.00
7.50
7.00
6.50
6.00
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Comp


TPLZ vs TEMP
AHCT245, B to A, Lot #1
Vcc = 4.5V
TPLZ (ns)
13.50
12.50
11.50
10.50
9.50
8.50
7.50
6.50
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Lot #1
TPLZ vs TEMP
AHCT245, B to A, Lot #2
Vcc = 4.5V
TPLZ (ns)
13.50
12.50
11.50
10.50
9.50
8.50
7.50
6.50
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Lot #2
TPLZ vs TEMP
AHCT245, B to A, Lot #3
Vcc = 4.5V
TPLZ (ns)
13.50
12.50
11.50
10.50
9.50
8.50
7.50
6.50
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Lot #3
TPLZ vs TEMP
AHCT245, B to A, Competitor
Vcc = 4.5V
TPLZ (ns)
13.50
12.50
11.50
10.50
9.50
8.50
7.50
6.50
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Comp


TPLZ vs TEMP
AHCT245, B to A, Lot #1
Vcc = 5.5V
TPLZ (ns)
11.00
10.50
10.00
9.50
9.00
8.50
8.00
7.50
7.00
6.50
6.00
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Lot #1
TPLZ vs TEMP
AHCT245, B to A, Lot #2
Vcc = 5.5V
TPLZ (ns)
11.00
10.50
10.00
9.50
9.00
8.50
8.00
7.50
7.00
6.50
6.00
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Lot #2
TPLZ vs TEMP
AHCT245, B to A, Lot #3
Vcc = 5.5V
TPLZ (ns)
11.00
10.50
10.00
9.50
9.00
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8.00
7.50
7.00
6.50
6.00
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Lot #3
TPLZ vs TEMP
AHCT245, B to A, Competitor
Vcc = 5.5V
TPLZ (ns)
11.00
10.50
10.00
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6.50
6.00
-55 -35 -15 5 25 45 65 85 105 125
TEMP (°C)
Comp

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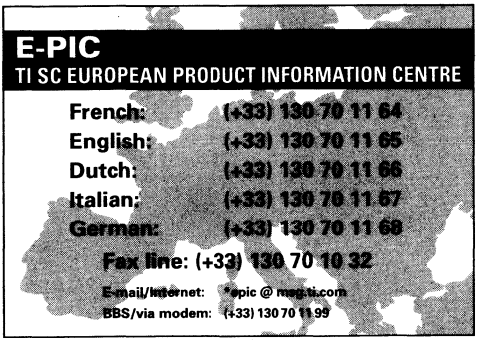

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Printed in Germany
Sellier Druck GmbH, 85354 Freising

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